ATA Memo 22

Generalization Of The Memoryless Corner Turner To The Non-Square Case

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Abstract

This memo describes how the memoryless corner turner architecture proposed by Urry [1] can be extended to handle the case where the number of input streams and the number of output streams are unequal, and where the input and output clock rates are also unequal.

Introduction

We define a "corner turner" as a device that performs a matrix transpose on data that is presented in serial form for one dimension of the matrix and in parallel form for the other. Specifically, it accepts N data streams in parallel at clock rate f_i, where each stream is itself a serialization of M streams at clock rate f_i/M. Each elementary unit of data is a word of length W bits, so the total input date rate is $f_i NW$. Then at the output of the corner turner the data has been reorganized so as to interchange the serial and parallel parts; that is, we have M data streams where each is a serialization of the N inputs that all correspond to the same sample $m \in \{0, \ldots, M-1\}$. The output clock rate is then $f_o = f_i N/M$, so that the total output data rate $f_o MW$ is the same as the total input data rate.

Urry [1] has proposed an efficient corner turner architecture for the special case of $N = M = 2^k$ for integer k, which we call the "square" case. It requires $N \log_2 N$ 1P2T switches toggling every input clock cycle, but it does not require any storage. Let such a device be called a "Urry Turner of size N." Here we describe how to extend this architecture so as to cover cases where $N \neq M$.

One subtlety of the Urry Turner is that it requires the input data to be skewed so that when stream n is presenting sample m, stream $n+1$ should be presenting sample $m+1$, for all streams modulo N. Given a data source where all samples of the same index are presented together, this requires a delay of n samples for stream n, where $n = 0, \ldots, N-1$. For this discussion, those delays are considered to be part of the Urry Turner, so that the input data presented on the same clock all have the same index. The output data will still be skewed in a similar way, but this will not affect our discussion.

Integer Ratio Cases

Consider first the situation where $N/M = 2$. Then we want half as many outputs as inputs, each at twice the rate. This can be handled by a single Urry Turner of size M operating at $f_o = 2f_i$ preceded by a bank of $N/2$ 1P2T switches as shown in Figure 1. The switches must toggle twice per input sample so as to present even and odd numbered input streams to the Urry Turner on alternate output clock cycles. This is equivalent to multiplexing pairs of input streams into one stream having twice as many samples per period. The scheme can be generalized to $N/M = K$ for integer K by using N/K 1PKT switches.

Next consider $M/N = 2$. Then there must be twice as many output as input streams, each at half the rate. This can be accomplished by using two Urry Turners of size N, each operating at rate $f_o = f_i/2$, preceded by a bank of N 1P2T switches where each toggles at rate f_i. The arrangement is shown in Figure 2. The idea is that all the even numbered input samples are handled by the first Urry Turner and all the odd numbered ones are handled by the second one. Again, this can be generalized to any $M/N = K$ for integer K by using K Urry Turners and 1PKT input switches.

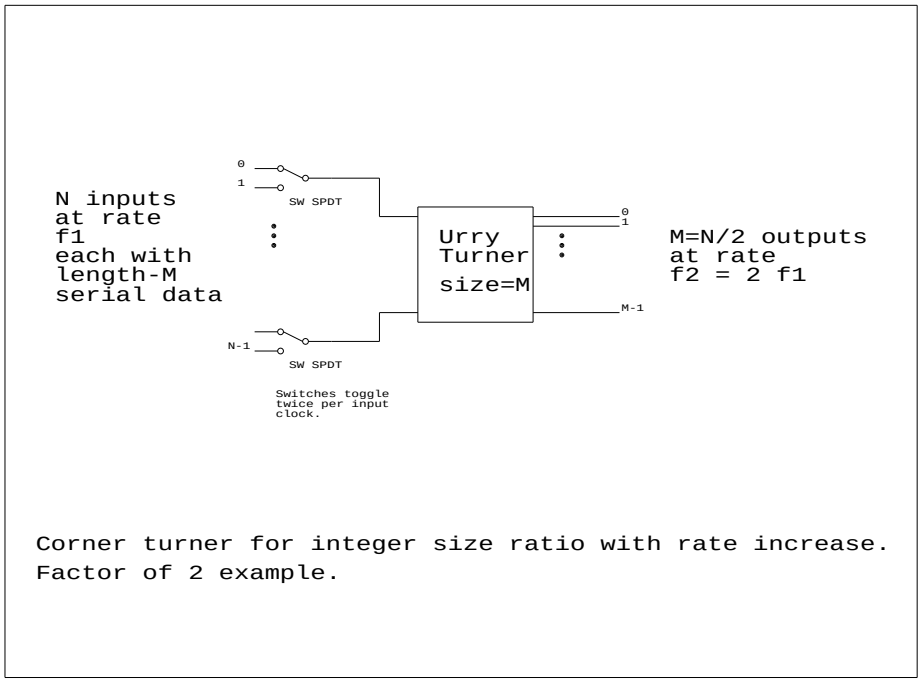

Figure 1 Corner turner for decreasing the number of streams and increasing the clock rate by a factor of 2.

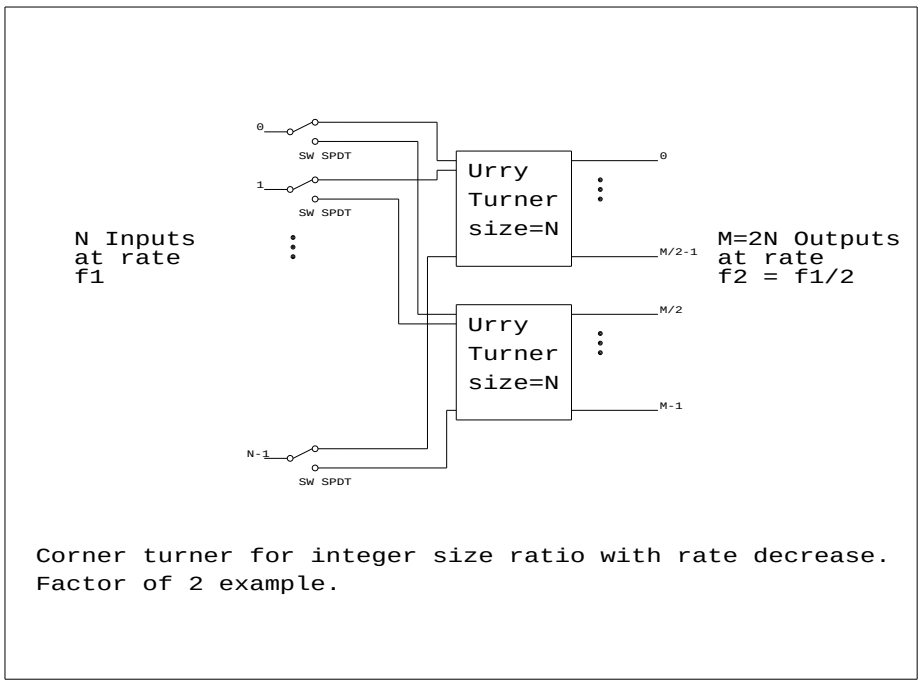

Figure 2 Corner turner for increasing the number of streams and decreasing the clock rate by a factor of 2.

Non-Integer Ratio Cases

Now let $M < N < 2M$, so that we wish to decrease the number of output streams by less than a factor of 2. Create $2M - N$ additional "dummy" input streams so that the total number of input streams becomes $N' = 2M$. Then proceed as in Figure 1 by time-multiplexing the $2M$ streams into

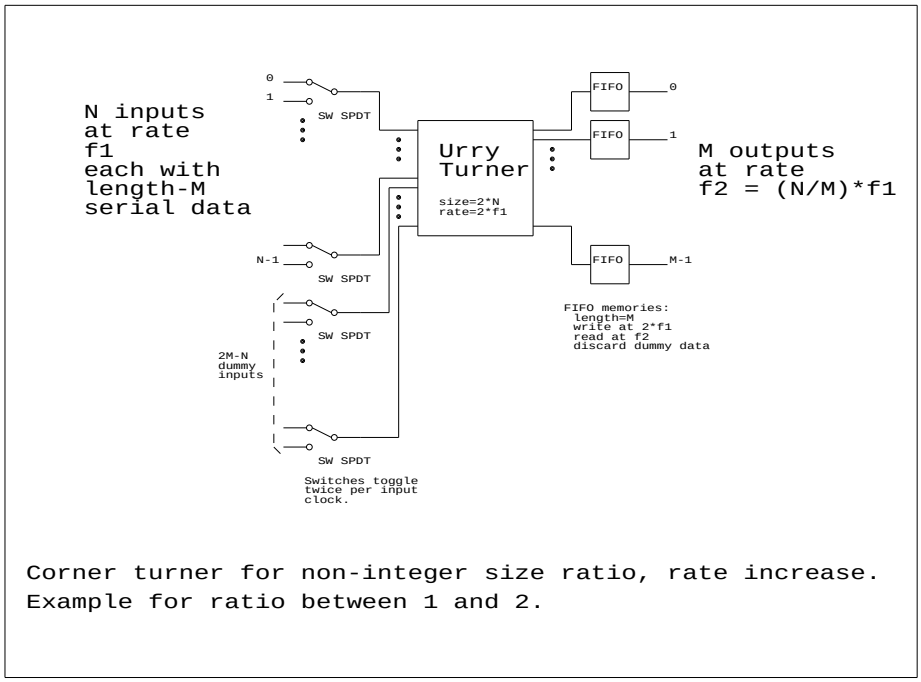

Figure 3 Corner turner for decreasing the number of streams and increasing the clock rate by a rational factor between 1 and 2.

M and supplying them to a Urry Turner of size M. We then have the correct number of outputs, but the clock rate is higher than desired and each stream contains some dummy data. Each output stream carries the sequence $n = 0, 1, \ldots, N-1$ followed by $2M - N$ dummy values. Each can be adjusted to the desired clock rate while eliminating the dummy data by writing it to a FIFO of length M at rate $2f_i$ and reading from the FIFO at rate $f_o = (N/M)f_i$. This arrangement is shown in Figure 3. It can be generalized to larger N/M ratios where $(K-1)M < N < KM$ by similarly creating fewer than N dummy inputs so as to "pad up" to the next integer multiple of M, namely $N' = KM$.

Finally, let $N < M < 2N$, so that we wish to increase the number of output streams by less than a factor of 2. To do this, we pad the input streams serially (rather than in parallel, as in the previous case). This is accomplished by having a FIFO of length $2N$ on each input stream, as shown in Figure 4. We write into this FIFO at rate f_i for M clocks, and then we read from it at rate $f_o = (N/M)f_i$ for $2N$ clocks; on the last $2N - M$ of these clocks, dummy values are read from the FIFO. We then proceed as in Figure 2 by routing alternate outputs of the FIFOs to two Urry Turners of size N. Of the $2N$ outputs from the corner turners, $2N - M$ will contain the dummy data, so they can simply be ignored. The remaining M outputs are the desired ones, and they are produced at the desired clock rate. Generalizing to larger ratios is straightforward, where the input length is padded up to the next integer multiple of the input width using a FIFO of that length and the corresponding number of size-N Urry Turners.

It should be noted that these corner turners are no longer memoryless, due to the presence of the FIFOs. But this memory is much simpler than in the more obvious implementation where the inputs are written serially at rate f_i into N shift registers of length M, the contents of these are copied in parallel to M orthogonal shift registers of length N, and those are shifted out at rate f_o.

REFERENCE

L. Urry, "A corner turner architecture." ATA Memo 14, 2000-Nov-17.

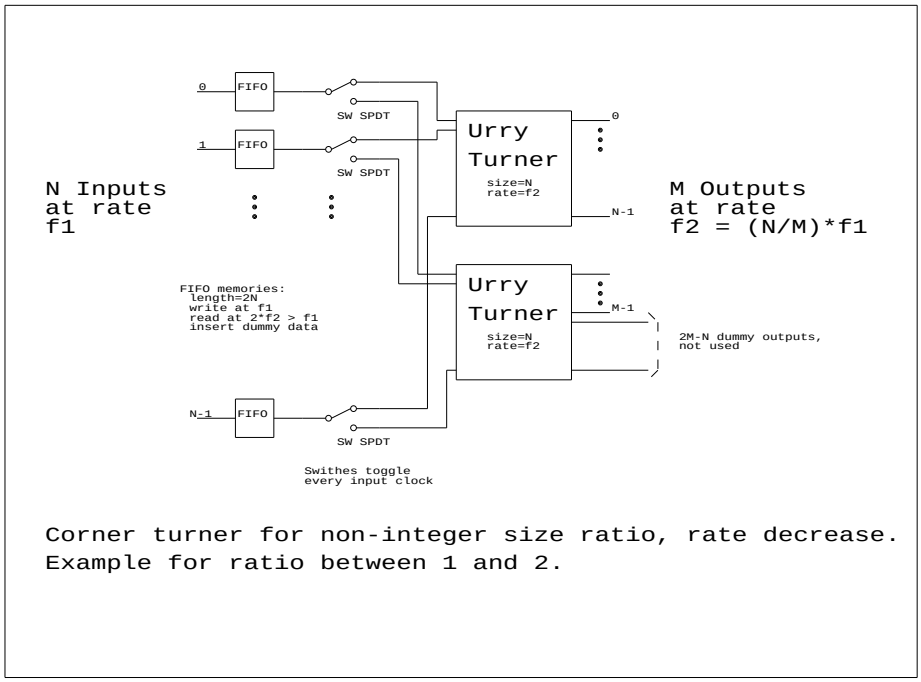

Figure 4 Corner turner for increasing the number of streams and decreasing the clock rate by a rational factor between 1 and 2.