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Digital Tests of Quadrature Downconverters

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In [1] I described measurements of the performance of certain quadrature downconverter chips using analog techniques. One of them, the MAX2108, has now also been characterized digitally, using the Digitizer Breadboard assembly that was described in [2]. The new tests are briefly reported here.

In these measurements, the I and Q signals were each digitized to 8b (nominal) at a rate of 125 MHz. A set of 2040 consecutive samples was captured into RAM and then transferred to a PC for analysis. All processing and plotting were done in MATLAB, partly using routines written for the purpose but also relying on the built-in functions `spectrum(c)` (for the frequency analyses) and `cov(x,y)` (for covariance matrix calculation).

The following parameters apply to all the measurements:

LO frequency: 2.000 GHz;
Input power to analog board: –7.9 dBm;
Gain control voltage: 3800 mV
Baseband lowpass filters: not installed.

See the Addendum of [1] for a discussion of signal level and gain. A separate set of samples was acquired at each of 20 baseband frequencies from –100 MHz to +100 MHz in steps of 10 MHz (except zero).

To estimate the quadrature error, the covariance matrix of the I and Q samples for each frequency was calculated as

$$x = \begin{bmatrix} < I^2 > & < IQ > \\ < QI > & < Q^2 > \end{bmatrix},$$

and then the gain, gain ratio, and phase error were derived as

$$\begin{aligned} g &= x_{11} + x_{22} \\ r &= \sqrt{x_{11}/x_{22}} \\ \delta\phi &= 0.5 \sin^{-1}(x_{12}/\sqrt{x_{11}x_{22}}). \end{aligned}$$

These results are plotted in the first of the following figures. The formulas are appropriate if only the desired signal is present, so that x_{11} and x_{22} measure its power. In the practical case where it is accompanied by noise and distortion, the gain is overestimated and the phase error is underestimated.

Next the covariance matrix X was calculated using *all* of the samples from frequencies of –50 to +50 MHz, so as to find the average error over that range. This was used to derive a correction matrix using

$$Y = \begin{bmatrix} r^{-1}\cos\delta\phi & -r\sin\delta\phi) \\ -r^{-1}\sin\delta\phi & r\cos\delta\phi \end{bmatrix}$$

where r and $\delta\phi$ were derived from X in the same way as for the single-frequency data. Then the corrected sample $\hat{s} = Ys$ was computed for every sample s, the errors were re-analyzed as before, and the results are plotted in the second figure. It can be seen that the correction had little effect on the phase error, since the uncorrected average error was nearly zero. The uncorrected amplitude imbalance was about 6% and it was corrected to less than 0.5%.

Spectra were also computed both before and after correction, and these are shown in the next two figures, respectively. The 10 plots in each figure cover baseband frequencies from –50 to +50 MHz. In each case the image response is reduced by the correction; at some frequencies it is reduced from about –30 dBc to undetectable (better than –45 dBc). It should be emphasized that the performance without correction was very good, with the worst image at about –28 dBc. In these plots, the left half is the upper sideband and the right is the lower sideband; the center ("1") is ±62.5 MHz, half the sampling rate. The strong central response is probably due to leakage of the half-clock signal generated within the ADC chips.

Finally, a new set of measurements was taken with the correction implemented in the FPGA of the breadboard. The same correction matrix Y derived from the first set of measurements was rounded to 8b (represented as [u8.8 s9.8; s9.8 u8.8] fixed-point numbers) and loaded into constant-coefficient multipliers. The correction was implemented with 8×8-bit multipliers and 12-bit adders, with the results rounded (not truncated) back to 8 bits. Number representations were carefully designed and the matrix elements were scaled to minimize loss of precision. Spectra derived from the new data are plotted in the fifth figure. It can be seen that the image response at every frequency is improved by about the same amount as in the MATLAB impleimentation.

The correction matrices were

$$\begin{bmatrix} 1.029783 & -.004568 \\ -.004568 & 0.971057 \end{bmatrix} \qquad \begin{bmatrix} 255/256 & -1/256 \\ -1/256 & 240/256 \end{bmatrix} = \begin{bmatrix} 0.9961 & -.0039 \\ -.0039 & 0.9375 \end{bmatrix}$$

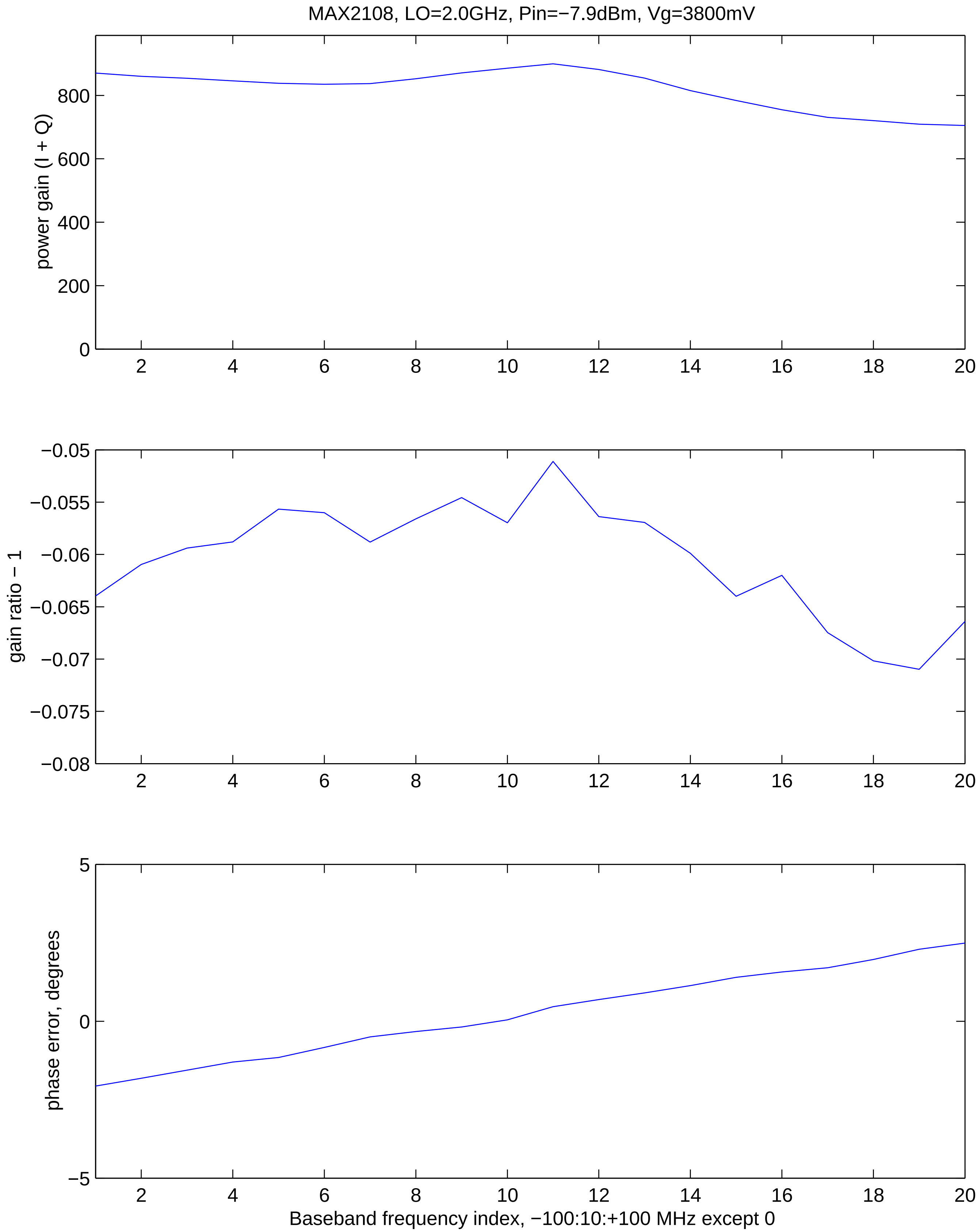
where the first was used for the MATLAB corrections (floating point), and the second was used in the FPGA corrections (8b fixed point).

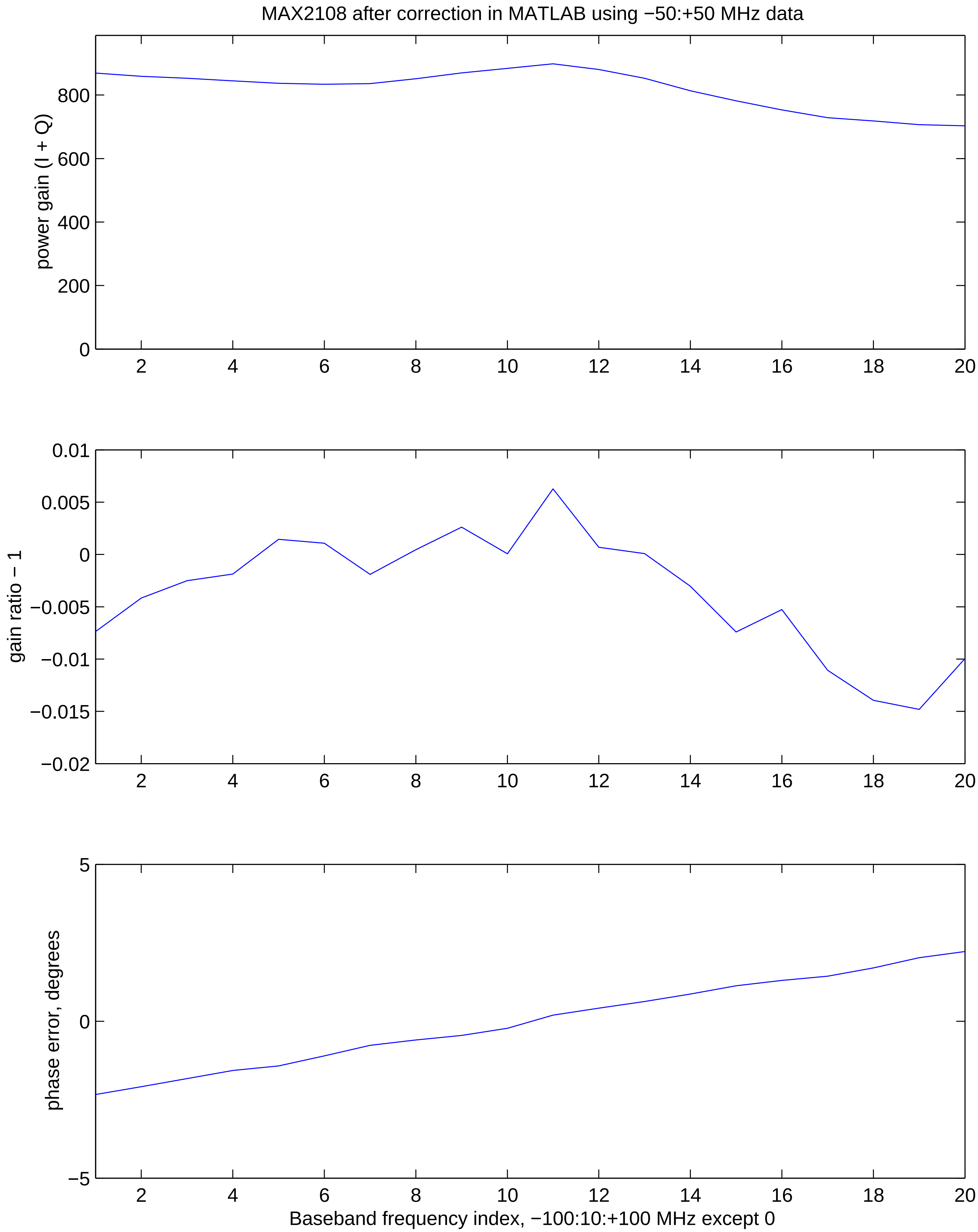
REFERENCES

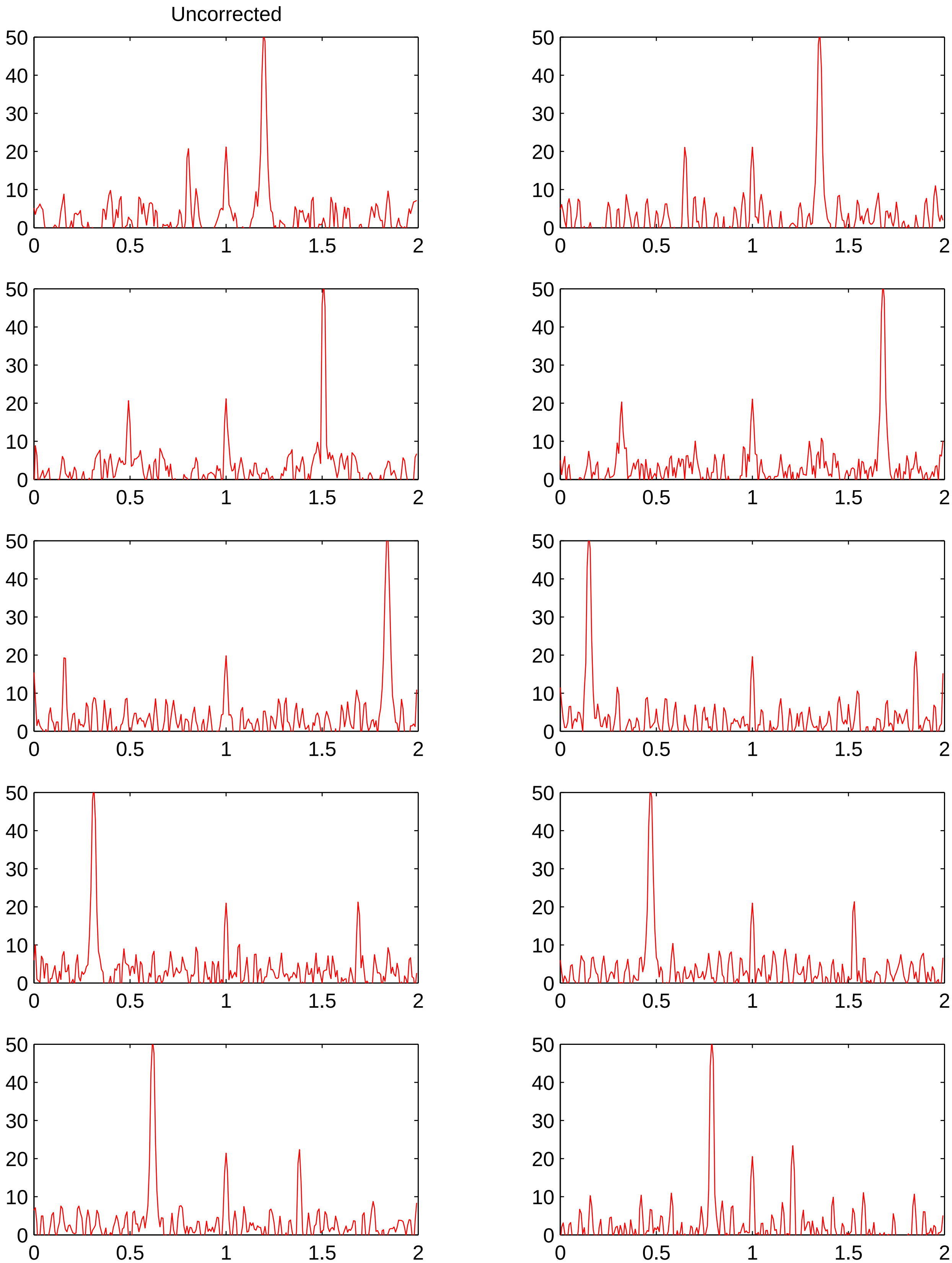
[1] L. D'Addario, "Performance tests of quadrature downconverters." ATA Memo No. 42, 2002-Jan-21.

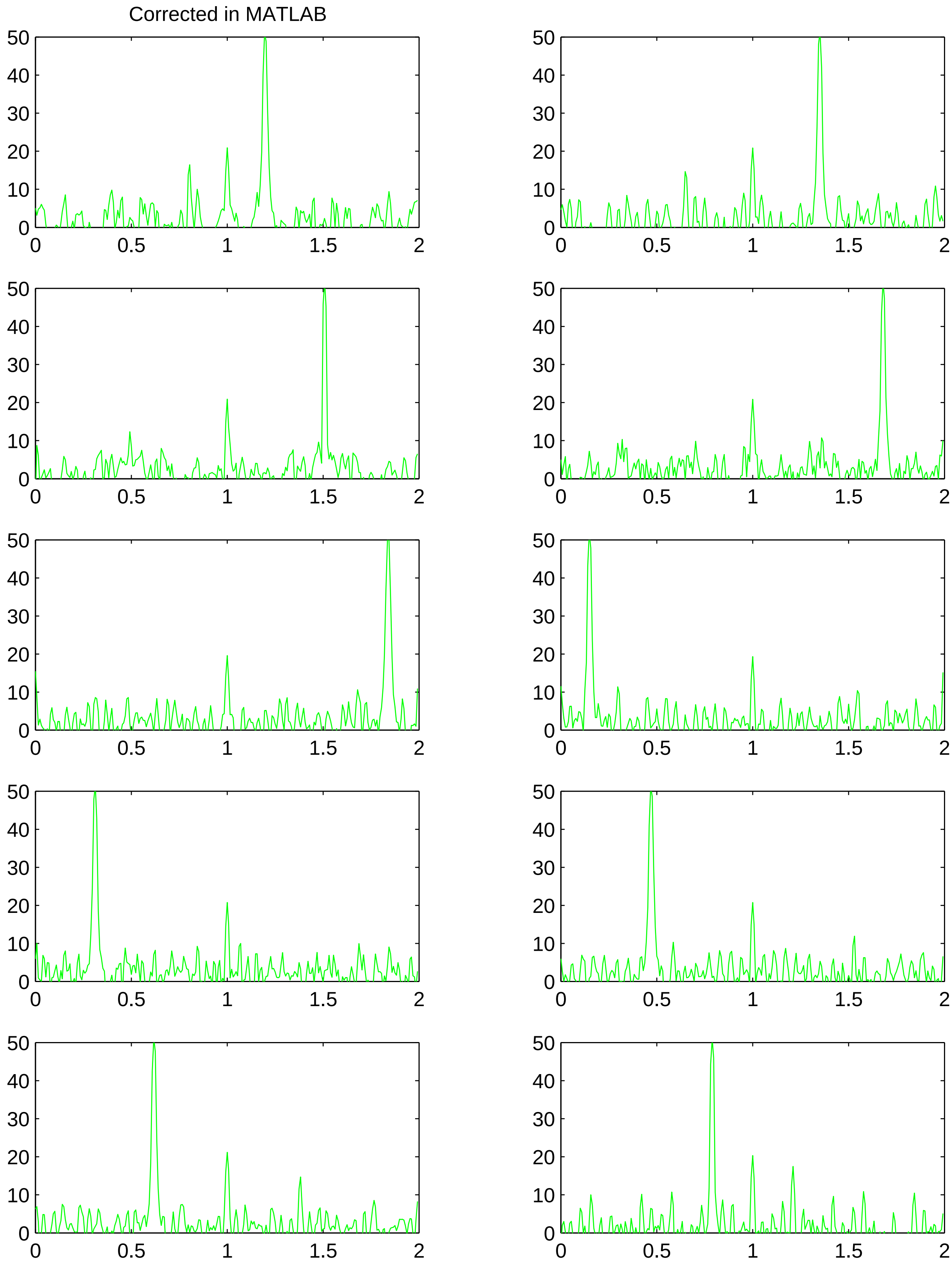
[2] L. D'Addario, "ATA digital subsystem: breadboard circuits." ATA Memo No. 41, 2002-Jan-20.

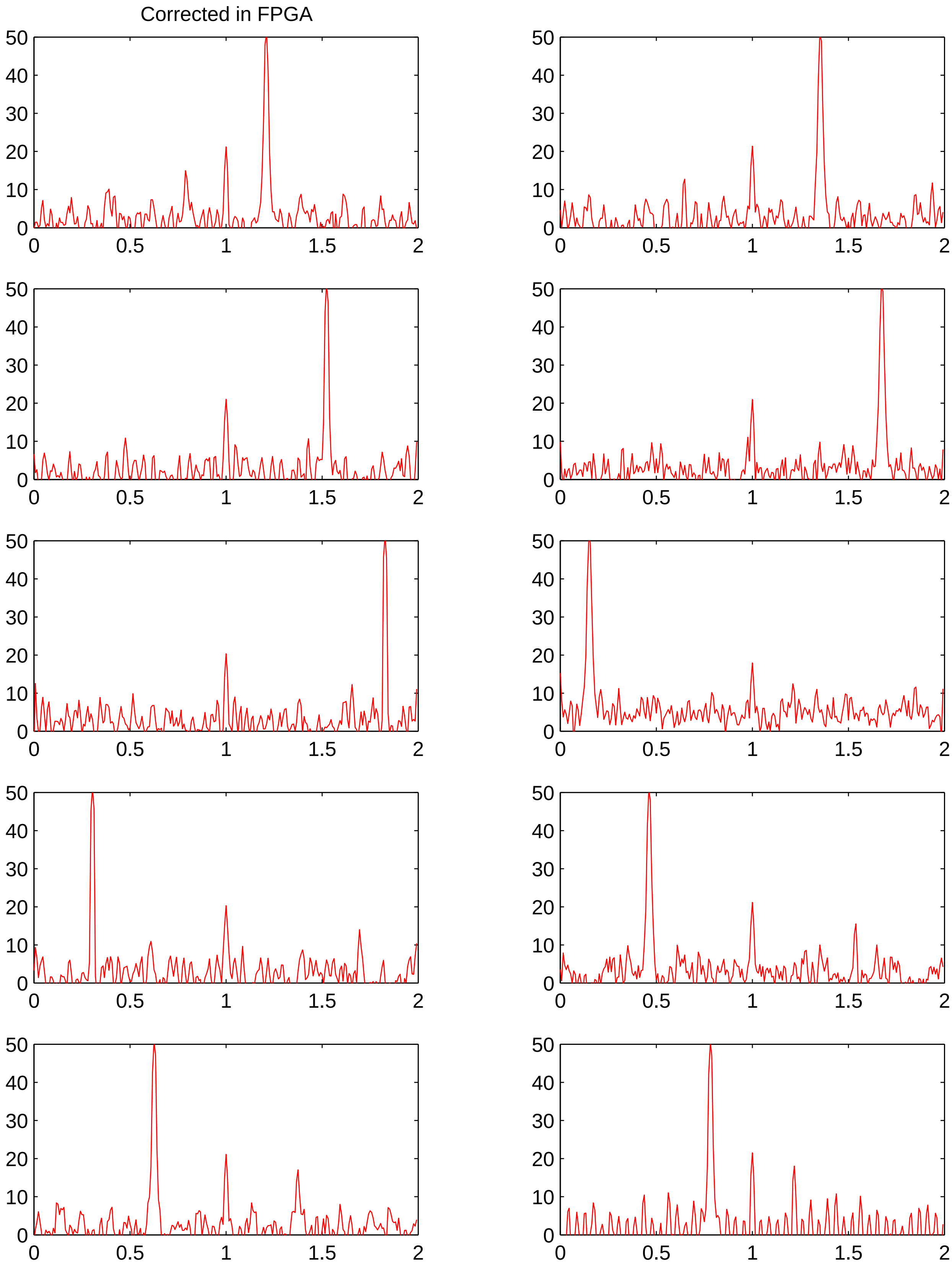
`http://intranet.seti.org/doc/ata/Memo`


MAX2108, LO=2.0GHz, Pin=−7.9dBm, Vg=3800mV
power gain (I + Q)
0
200
400
600
800
2
4
6
8
10
12
14
16
18
20
gain ratio − 1
−0.05
−0.055
−0.06
−0.065
−0.07
−0.075
−0.08
phase error, degrees
5
0
−5
Baseband frequency index, −100:10:+100 MHz except 0


MAX2108 after correction in MATLAB using −50:+50 MHz data
power gain (I + Q)
gain ratio − 1
phase error, degrees
Baseband frequency index, −100:10:+100 MHz except 0


Uncorrected
50
40
30
20
10
0
0.5
1
1.5
2


Corrected in MATLAB


Corrected in FPGA