ATA Memo No. 41

ATA Digital Subsystem: Breadboard Circuits

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2002 January 20

Introduction

In order to explore some of the technologies needed for the ATA's digital signal processing, a series of "breadboards" or test circuits has been constructed. A set of functions similar to those needed in the telescope is implemented in these circuits, but various simplifications have been made in order to allow the development to proceed quickly. Consequently, these circuits cannot be used directly as prototypes.

Components used in the breadboards were selected because they are candidates for use in the final design, but they are by no means the only candidates nor necessarily the best choices. The ATA's development schedule constrains us to use commercial off-the-shelf (COTS) components wherever possible. In most of the critical areas of this design – including analog to digital converters, FPGAs, and devices supporting fast optical links – new components are frequently introduced and the prices of known components may change in either direction. Thus, all selections must be carefully reviewed during detailed design of the prototype.

Summary Description

A block diagram of the suite of boards is shown in Figure 1.

First we have a two-board set that approximates the Digitizer Module planned for the telescope, consisting of "analog" (quadrature downconverter and filters) and "digital" (digitizers, FPGA, and serializer) assemblies. The analog board accepts a single 1–2 GHz IF channel and converts it to in-phase and quadrature (I and Q) baseband signals. The digital board digitizes the I and Q signals and passes the samples via the FPGA to the serializer, where they are formed into a single bit stream at approximately 2.5 Gb/s. Some processing can be carried out in the FPGA, but it is included mainly to facilitate testing. Since this was the first digital breadboard built, it has allowed early experimentation with FPGA coding and timing.

The fast serial bitstream then goes to a commercial laser driver board from Maxim Semiconductor where it modulates an 850 nm VCSEL from Honeywell. (In the prototype Digitizer Module, the laser and its driver should be integrated onto the digital board, and it is likely that two or more channels will be handled by one module.)

An optical fiber patchcord brings the signal to the final board of this suite, called the Receiver Breadboard. This is a partial and simplified approximation of the IF Processor Module planned for the telescope. It includes a Honeywell photodiode to demodulate the optical signal, followed by a deserializer IC to recover the parallel-word data samples. Two such channels are included on the board, similar to what is planned for the IF Processor, even though the digitizer breadboards provide only one channel. The recovered samples go to an FPGA for processing. This FPGA (a Xilinx Spartan-II with about 200k gates) is probably not large enough to implement all the processing required for the telescope, but it allows experimentation with each of the most critical functions. The processed data is available in word-serial form at a connector driven by the FPGA.

Each FPGA is accompanied by a flash EPROM designed to load the FPGA's programming automatically upon power-up. The EPROM can in turn be written via a JTAG port, and the FPGA can also be loaded directly via this JTAG port.

The initial programming of each FPGA includes a control/monitor interface that can connect to the parallel port of a PC. Among other things, it allows 2048 signal samples to be captured at full speed into the FPGA's RAM and then dumped more slowly to the PC for further analysis. It should be emphasized that this interface is quite inadequate for operating the actual modules of the telescope; it is one of the simplifications made to allow rapid development of the breadboards. (In the prototypes, an on-board microcontroller is expected to be needed, with the interface to the telescope's command/monitor system implemented there.)

The following sections of this report describe the various assemblies in more detail. It will be assumed in the discussion that the reader has access to the manufaturer's data sheet for each of the components.

Digitizer: Analog Board

Figure 2 is a schematic of the analog board. Its main component is a Maxim MAX2108CEG quadrature downconverter IC. The good performance [1] and low cost ($4.63 each in quantity) of this device makes feasible the planned digitizer architecture. Its input range is 950 to 2150 MHz, so it can be used anywhere in the 1–2 GHz IF of the telescope. Unlike some of the other components of the breadboards, we know of no reason not to adopt this device for the prototypes.

Unfortunately the RF and LO inputs of the MAX2108 are poorly matched, so the board includes resistive padding on each. We want to operate the input interface from the RF-IF converter at a relatively high power level in order to minimize the effects of spurious signals [2], and even though we choose to operate the MAX2108 near its minimum gain this still requires about 20 dB of padding at the RF port. The full-scale input level is intended to be +10 dBm within the 100 MHz output bandwidth, but the normal level for the system noise should be 27 dB lower (–17 dBm in 100 MHz or –7 dBm in 1 GHz for white noise). The LO input has a 5 dB pad, so –5 to 0 dBm is needed at the board's SMA connector.

The MAX2108 includes a variable-gain RF amplifier with 50 dB of range. The levels are chosen to allow it to be operated near its minimum gain for best temperature stability. Tests [1] and calculations show that the noise figure and harmonic distortion are adequate. Nevertheless, about 10 dB of the gain adjustment range is intended to be available in the system to take up gain tolerances elsewhere and to allow for variations in system temperatures. A DAC is provided on the breadboard to drive the gain control. The board layout actually provides space for two different DACs, only one of which should be installed. A dual DAC is used because the prototype boards are expected to include at least two channels, even though the breadboard has only one. The present board uses the Burr-Brown (TI) DAC7602, but the Maxim MAX5104 has some price and performance advantages. Both have serial data interfaces. A LabView program has been successfully written to control the DAC7602 via a PC's parallel port (for Win98 or earlier only). A C program to do the same thing has been written but not yet debugged. Tests show that gain resolution of about .04 dB is possible.

The baseband outputs of the MAX2108 are connected to a set of lowpass filters that provide alias rejection for the ADCs that follow (on the next board). The board layout allows us to try several types of filter. The MAX2108 outputs use differential signals, and most high-speed ADCs have differential inputs, so provisions were made for differential-mode filters. Pads are provided on the board for construction of these filters from discrete chip inductors and chip capacitors, with space for a 4-section symmetrical (9 pole) elliptical-function design. A separate breadboard (not further discussed here) was built to test such filters using off-the-shelf Ls and Cs of 2% tolerance, but the initial results were not good and the effort was abandonded. (If this approach can be perfected, it will result in substantial cost savings compared to alternatives.) The board also contains provisions for mounting LPFs procured from Lark Engineering [3,4], part number LMS802-687. These are 50 ohm single-ended filters used in pairs as 100-ohm differential filters. It is important to remember that the Lark filters were purchased as matched pairs that ought to be kept together. This was intended to match the I and Q signal paths for better image rejection, not to match the two sides of a differential pair.

The MAX2108 data sheet claims differential output impedance of 33 ohms and a saturation level of 1.5V p-p, but tests show significant distortion at lower levels. To ensure adequate drive at the full-scale ADC level of 1 V p-p, differential buffers (Analog Devices AD8131AR) are used. These provide a fixed voltage gain of 2.0 at an input impedance of 1.5k.

The differential outputs of the board are on pairs of SMA connectors. The layout includes a provision for an optional transformer to convert to single-ended 50 ohm outputs, so as to allow convenient stand-alone testing. Either the differential connectors or the transformer plus single-ended connector should be installed, not both. Additional discussion of options for interconnection with the digital board is given in the next section.

The board operates on a single +5 volt supply.

Digitizer: Digital Board

Figure 3 is a schematic of the digital board.

Input Circuits

Differential inputs for the I and Q signals are provided on pairs of SMA connectors. These are coupled to two ADCs via transformers, which provide a means of setting the d.c. offset to mid-scale. Although a direct connection without transformers would be possible, it is desirable to avoid d.c. coupling because of the many opportunities for introduction of spurious signals at or near d.c. (This produces a notch in the frequency response at zero frequency, which is the center of the observed band. This is considered acceptable in our astronomical application, but it would not be acceptable in many communications applications.) To allow convenient testing of the board in a stand-alone manner with single-ended 50 ohm inputs, provisions are included for shorting one side of the transformer primary to ground and adding a 100-ohm resistor in parallel.

High-speed ADCs are often provided with differential inputs in order to cancel common-mode spurious signals such as pickup of the clock. In our system, we would like to take advantage of this as much as possible, especially if the prototypes (like the breadboards) should separate the analog and digital circuits onto separate boards. In that case, the interconnection between boards should be differential. However, the use of differential anti-aliasing filters can be expensive; standard commercial filters are single-ended, so either a high-cost special design or twice as many single-ended filters must be used. Therefore, the presently-favored design is a bit different from these breadboards. In that design, illustrated in Figure 4, single-ended LPFs are used for I and Q on the analog board, followed by transformers there to convert to differential and to provide d.c. isolation. The digital board then connects the differential signals directly to the ADCs with a 100-ohm differential termination but no other coupling components. This topology can be implemented with the present boards by small modifications, except that the transformer is located on the digital rather than the analog board and the interconnection is single-ended.

Analog To Digital Converters

The ADCs are Signal Processing Technology type SPT7722 ICs. They have 8b resolution and are capable of sampling rates up to 250 MHz. As of this writing, the author believes that these are the best available devices for sampling rates of 150 to 250 MHz. If the final design requires only lower sampling rates, say around 125 MHz or less, competing devices may be better and/or cheaper.

The board provides two options for supplying the clock signal to the ADCs: from an external sinusoidal signal at -10 dBm or more via an SMA connector (J5) and MC100EL receiver; or from the FPGA. Jumper wires must be soldered to pads on the board to select one of these (J2 to J3 or J4, J6 to J7 or J8). Using the external clock allows testing at sampling rates higher than the FPGA might be able to provide, and it also allows the sampling phase to be adjusted relative to that of the FPGA's clock.

The ADC outputs normally operate in a ping-pong manner, alternating samples between two output busses so as to limit the rate on each pin to half that of the clock. There is a single-bus output mode available, but only for sampling rates of 125 MHz or less; the board has no provision for selecting this mode. There is also a two-bus mode in which the current and preceding samples are presented simultaneously, rather than alternately; this can be selected by soldering a jumper wire between pads provided on the board (P2-P3 and P5-P6). There is also a high-speed differential input for resetting the output divider to a known state, in case it is necessary to force a particular sample to be on one bus or the other. This is driven by the FPGA, but its use is not necessary because an ADC output signal ("DCLKOUT") always tells the FPGA which bus has the latest sample. All output signals from the ADCs are wired to FPGA inputs.

The ADCs require separate power and ground for the analog and digital sides. The board is constructed with a split ground plane on layer 2, where the two sides are connected only by a ferrite bead inductor (L2). There is a corresponding split power plane on layer 3, with +5V for the analog side on one part and +3.3V for the digital side on the other. The digital supply may have any value from 3.3 to 5.0V, but 3.3V is chosen for compatibility with the FPGA.

FPGA

A Xilinx Spatan-II series FPGA was chosen for low cost, but the largest available device in the series (200k gates) was selected to allow maximum flexibility in experimenting with processing algorithms. A quad flat package was chosen to allow probing at the pins, even though the same chip is available with more I/O pins in BGA packages; the 208 pin QFP provides more than enough I/O for our purposes. This series uses 2.5V power for its core logic, but it accepts various supply voltages and supports various standards at its I/O blocks. When the board was layed out, 3.3V was used for most pins but an option to use either 3.3V or

2.5V on two banks of pins was provided by a jumper. Those banks were intended for connection to the 2.5V serializer chip. However, it was later discovered that all I/O power pins are connected together internally for this package (unlike the larger packages for the same chip), so the jumper must always be left in the 3.3V position. Fortunately, the serializer chip is compatible with 3.3V LVTTL signals.

To keep the number of board layers to 4 (and thus reduce the cost and time of fabrication), the 2.5V power was not assigned to a separate plane but rather was run in thick lines and pours on layer 4. Elsewhere, layer 4 is used for signal wires when necessary for crossovers; as much as possible, signal wires are confined to layer 1.

The board supports several options for configuration of the FPGA. First, it includes a Xilinx flash EPROM (XC18V02, 2 Mb) wired so that its contents are automatically loaded into the FPGA upon power-up (provided that certain jumpers are installed). Second, the FPGA can be configured via a JTAG port; the EPROM can be written from this same port since the two chips form a JTAG chain. Finally, the FPGA can be configured from an external serial source using either its master serial or slave serial mode. The JTAG port is at pins 7–10 of configuration connector J8, and the external serial port is at pins 1–8 of the same connector. The configuration mode is set by jumpers at P7 and P8, as summarized in Table 1.

Table 1: Configuration Mode Jumpers

	J7:1-2	**J7:3-4**	**J7:5-6**	**J8:2-3**
Master serial auto from PROM	YES	YES	YES	YES
Master serial external	YES	YES	YES	NO
Slave serial external	NO	NO	NO	NO
JTAG	X	X	X	X

The FPGA's clock can be supplied from a sinusoidal source at –10 dBm or more at an SMA connector (J9). It is squared up by an MC100EL LVPECL receiver, then level-shifted in an RC network for compatibility with the 3.3V LVTTL input of the FPGA. The signal is connected to one of the FPGA's dedicated clock inputs.

Two connectors are provided for general-purpose, usually low-speed I/O to the FPGA. The first (J15) has 8 pins from FPGA I/O and 8 adjacent ground pins, and is intended for configuration jumpers to provide static mode information. It can also be used to bring out internal signals for probing. The other (J16) has 10 pins connected to FPGA I/O plus power and ground. It is intended to provide an 8b bi-directional data port and two control lines for connection to an external computer. This port is supported by existing FPGA logic and a PC program (see Appendix B), via the PC's parallel port. It is possible to set internal control bits of the FPGA and control bits of the serializer; to monitor internal status bits; to read and write a 16x2048b FPGA RAM; and to trigger capturing of samples into the RAM.

Finally, 16 output pins from the FPGA are wired to the 16b transmit data bus of the serializer and one is wired to its reference clock input. Generally these are just passed through the FPGA from the two 8b samples of the ADCs, but some processing can be done along the way. The FPGA also drives 5 control lines of the serializer; these set its operating mode.

Serializer

A Texas Instruments TLK3101 IC is used to convert the 16b data words into a single serial bitstream. It was chosen for this breadboard primarily because it was readily available from stock and relatively inexpensive ($48.38 in small quantities). Various competing devices may be better for the prototype. The TLK3101 has some undesirable features, such as fixed encoding of the data that cannot be disabled nor bypassed; but it also has features that are very convenient for early development, such as built-in generation and detection of a pseudo-random bit sequence.

The device uses 8b/10b encoding [5,6], so each 16b input word produces 20b of output at a rate of 20 times the input clock. It accepts input clock rates of 125 to 156.25 MHz, producing output rates of 2.5 to 3.125 Gb/s. (A pin-compatible chip, TLK2711, works at output rates of 1.6 to 2.7 Gb/s.) The device is actually a transceiver, so it includes complementary de-serializing and decoding logic; here we are using the transmitting side only, and the receive data bus is left unconnected.

The high speed output of the IC is supplied as differential LVPECL, capable of driving 50 ohm lines (100 ohms differentially). It should be a.c. coupled unless directly driving the high speed inputs of another TLK3101. On this board, we have connected the outputs directly to a 100 ohm differential line terminated in a pair of SMA connectors.

Laser Board

This board is part of the Maxim MAX3287SWEVKIT, an evaluation kit for some of their laser driver chips. We have configured it to use the MAX3297 IC, which supports 2.5 Gb/s transmission for common-cathode laser+photodiode devices.

A VCSEL (vertical cavity semiconductor laser) device from Honeywell, the HFE4191-521, has been installed on the board. This is a 2.5 Gb/s laser with photodiode, and is one of the only such devices that we could obtain quickly. It has a built-in and optically-aligned sleeve for mating with an LC-style fiber connector. This device is available in a duplex housing with a compatible optical receiver, so as to make a transceiver; that part number is HFT2191-521. The receiver is also available separately (HFD3380-102) in exactly the same package as the VCSEL. We have obtained four of these tranceivers as samples, but specially re-packaged as two VCSELs or two photodiodes in each assembly. In order to fit the assembly onto the Maxim board without excessive lead lengths, one of the VCSELS was removed from the outer package.

The board has several jumpers and pots that must be set according to the instructions provided on the data sheet. There is a configuration for testing the board without a laser (using laser-simulation components installed on the board), and this has been done successfully. The board was then configured for the laser and the Honeywell VCSEL was installed. As of this writing, the assembly has not been tested.

Receiver Board

The schematic is given in Figure 5.

This board supports two optical receiving channels at 2.5–3.125 Gb/s each. As explained in the previous section, we obtained samples of the Honeywell HFD3381-102 optical receiver (containing a photodetector and integrated preamplifier) with two units in one housing. The dual receiver is clamped to the edge of the PC board and each output is connected to a 100 ohm differential line. These lines go via d.c. blocking capacitors to the differential inputs of two TLK3101 ICs, the same devices as the one on the digitizer's digital breadboard but here used for receiving as a de-serializer and decoder.

The 16b recovered data word and word clock from each de-serializer are connected to input pins of the FPGA. This is the same type of FPGA as on the digitizer's digital board (Xilinx XC2S200), and many details of its integration onto the board are copied. The same configuration modes are supported in the same ways. General I/O connections for mode jumpers and/or probing (J15) and for interfacing to a PC (J16) are also the same, except that two additional control lines are provided on the PC interface connector. A clock signal for the FPGA is brought in via an SMA connector and MC100EP receiver, also the same as on the other board.

A total of 26 I/O pins of the FPGA are wired to a separate connector (P1), primarily for use as outputs of processed data samples. This is not enough to simulate an actual 2-channel IF processor, but it is sufficient for demonstration of the required functions. As mentioned in the summary section, the FPGA is also likely to be too small to implement all the required functionality; it is intended to support algorithm development and tests.

REFERENCES

[1] L. D'Addario, "Performance tests of quadrature downconverters." ATA Memo No. 42, 2002-Jan-21. `http://intranet.seti.org/docs/ata/Memo`

[2] L. D'Addario, "IF Power Level Specification (RF-IF Converter to Digitizer Interface)." Notes dated 2001-09-04.

[3] L. D'Addario, "Anti-aliasing filter." SETI Institute specification ATA.IFP.2001.1, 2001-May-31. tt http://astron.berkeley.edu/∼ldaddari/ata/filterSpecs.pdf

[4] Lark Engineering Quotation No. 9003, dated 09/19/2001; copy at: `http://astron.berkeley.edu/∼ldaddari/ata/larkEngineeringQuote.pdf` .

[5] L. D'Addario, "Notes On 8b/10b Coding for Serial Data Transmission," Report dated 2001-Aug-09. `http://astron.berkeley.edu/∼ldaddari/ata/8b10b.pdf` .

[6] A. Widner and P. Franaszek, 1982, "A d.c.-balanced, partitioned block, 8B/10B transmission code." *IBM J. of Res. Dev.*, vol 27, pp 440–451.

Appendix A — Construction Notes

The detailed layout of all boards was carried out by Calvin Cheng using the Protel 99 PCB software. Fabrication of the 4-layer boards was done by PCB Express (ECD, Inc. of Mulino, OR; `http://www.pcbexpress.com`), using their "Express 3" process with four day turnaround.

Schematics, layouts, and fabrication files are in Protel 99 "databases" named `digitizerBreadboard.ddb` for both the analog and digital boards of the digitizer; and `receiverBreadboard.ddb` for the receiver.

Appendix B — PC Program Notes

Programs `xpp.exe` ("Xilinx Parallel Port") and `app.exe` ("Analog board parallel port") have been written in C for communicating with the boards. These programs can be compiled with the Borland C/C++ or Xytec C compilers. The executables run under MS-DOS or in a "command" window under Windows98 or an earlier operating system. They will execute but will not function correctly under later versions of Windows because those opertating systems do not allow direct access to the parallel port.

The programs rely on DOS-specific (non-ANSI) library routines `inp()` and `outp()` for reading or writing an I/O port; and `kbhit()` for determining whether the keyboard buffer is empty.

The programs accept simple commands from the user. For the analog board, `app` merely sets the DAC to an typed value in millivolts. For the other boards, `xpp` has several commands for communicating with the bi-directional port implemented in the Xilinx FPGA. The command 'h' or 'H' or '?' lists the syntax of each available command.

There is also a LabView program with functionality similar to `app`, for setting the serial DAC on the analog board. It too works only under Windows98 or earlier.

NOTE: PDF versions of this document should have five more pages after this one, containing the figures. They are in the order 1, 4, 2, 3, 5. This is to facilitate printing, since the main text and Figures 1 and 4 are intended for A size paper, whereas Figures 2, 3, 5 should be printed on B size paper (11 by 17 inches) for legibility.

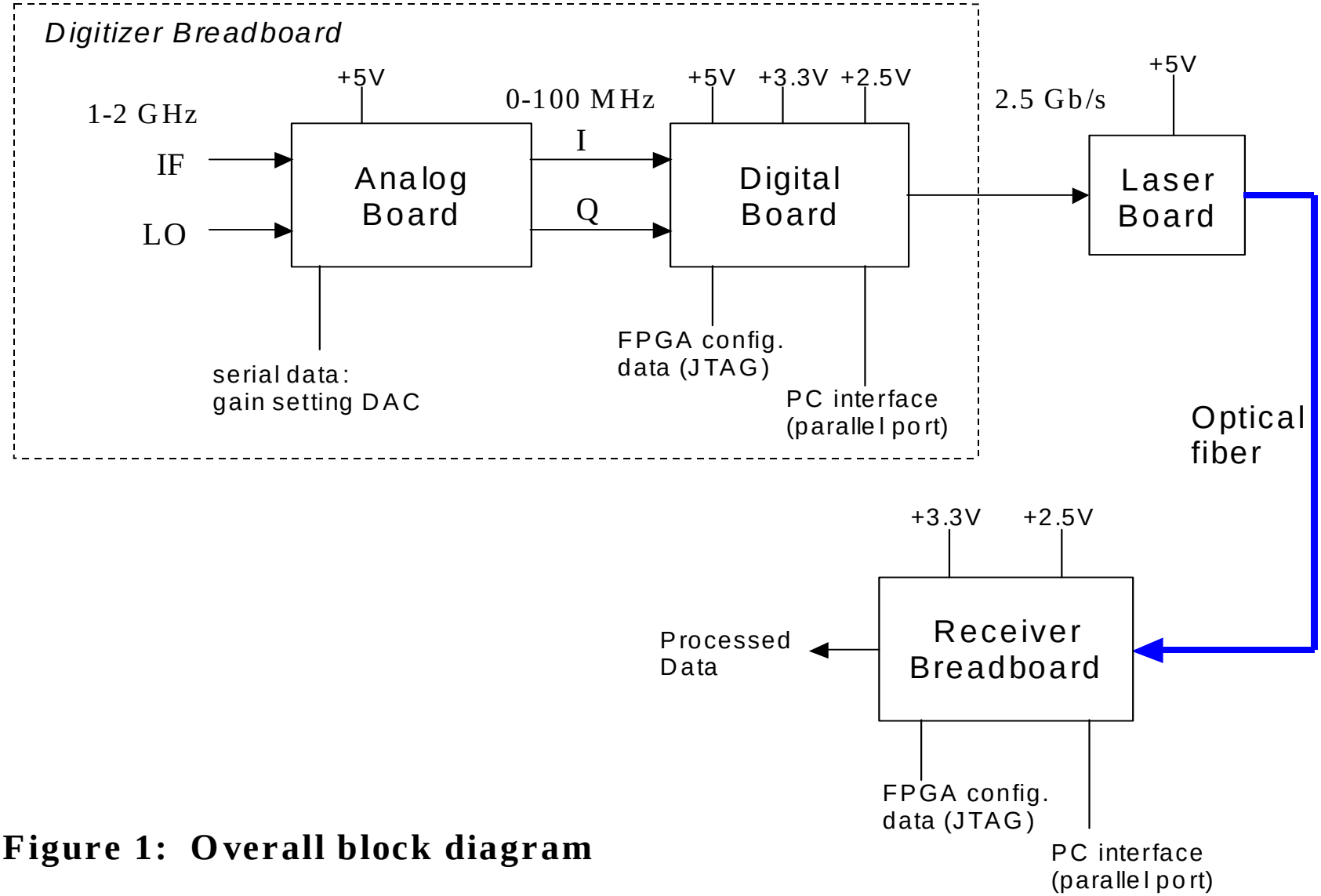


Figure 1: Overall block diagram

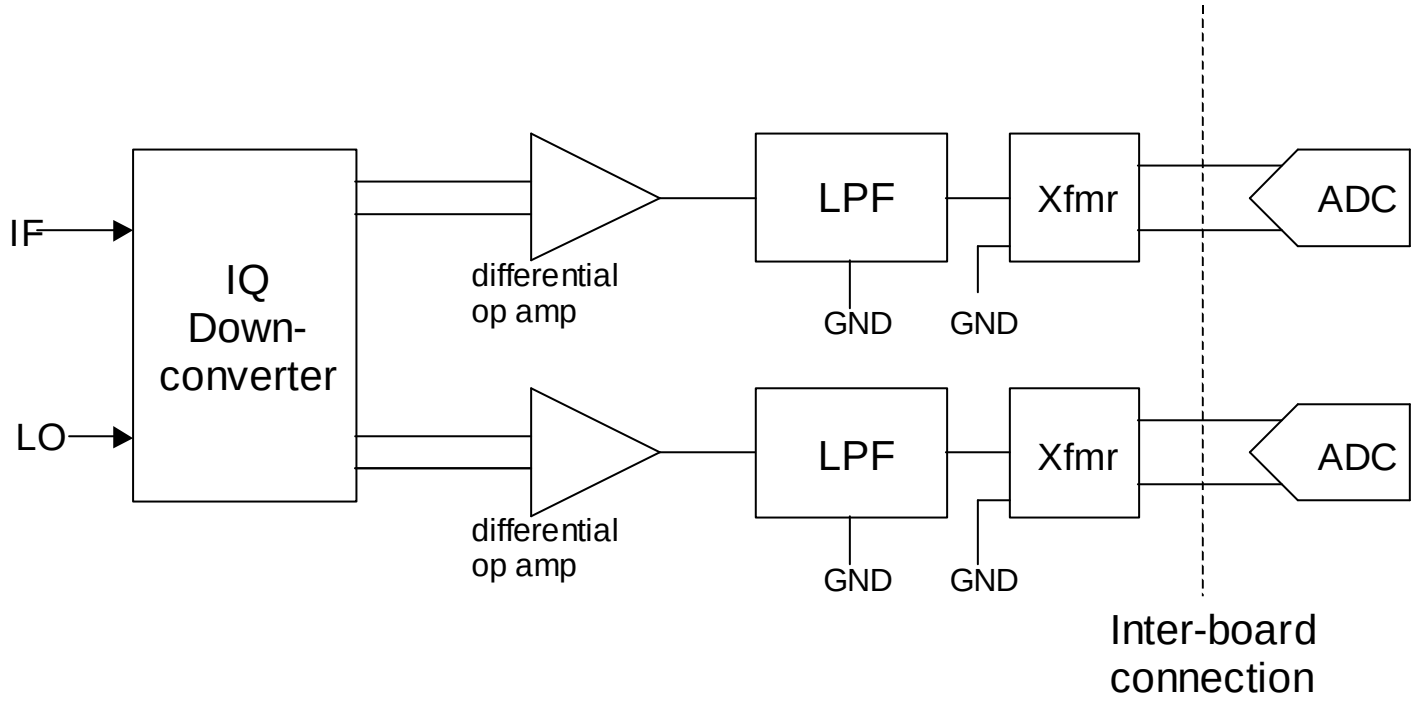
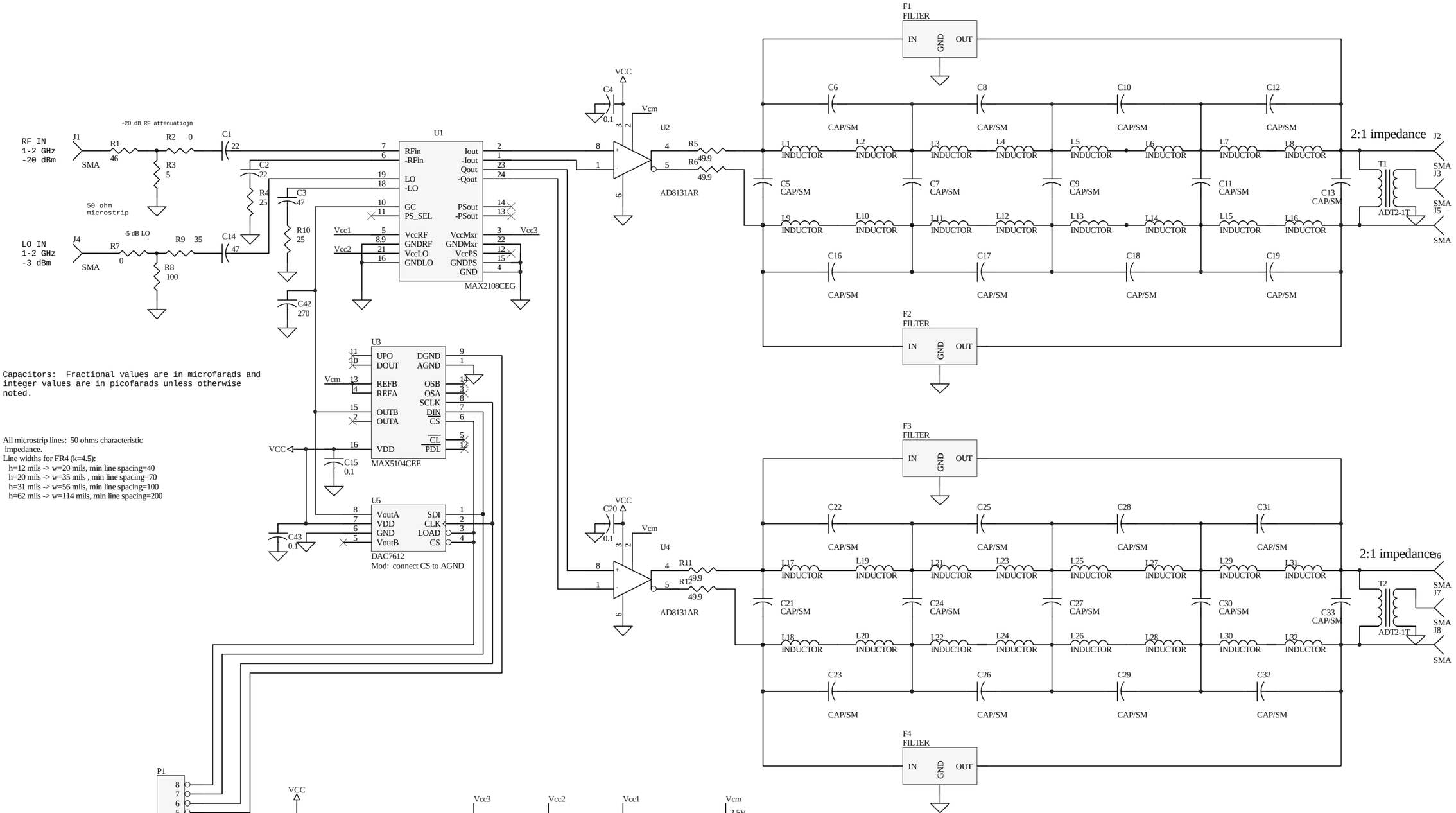
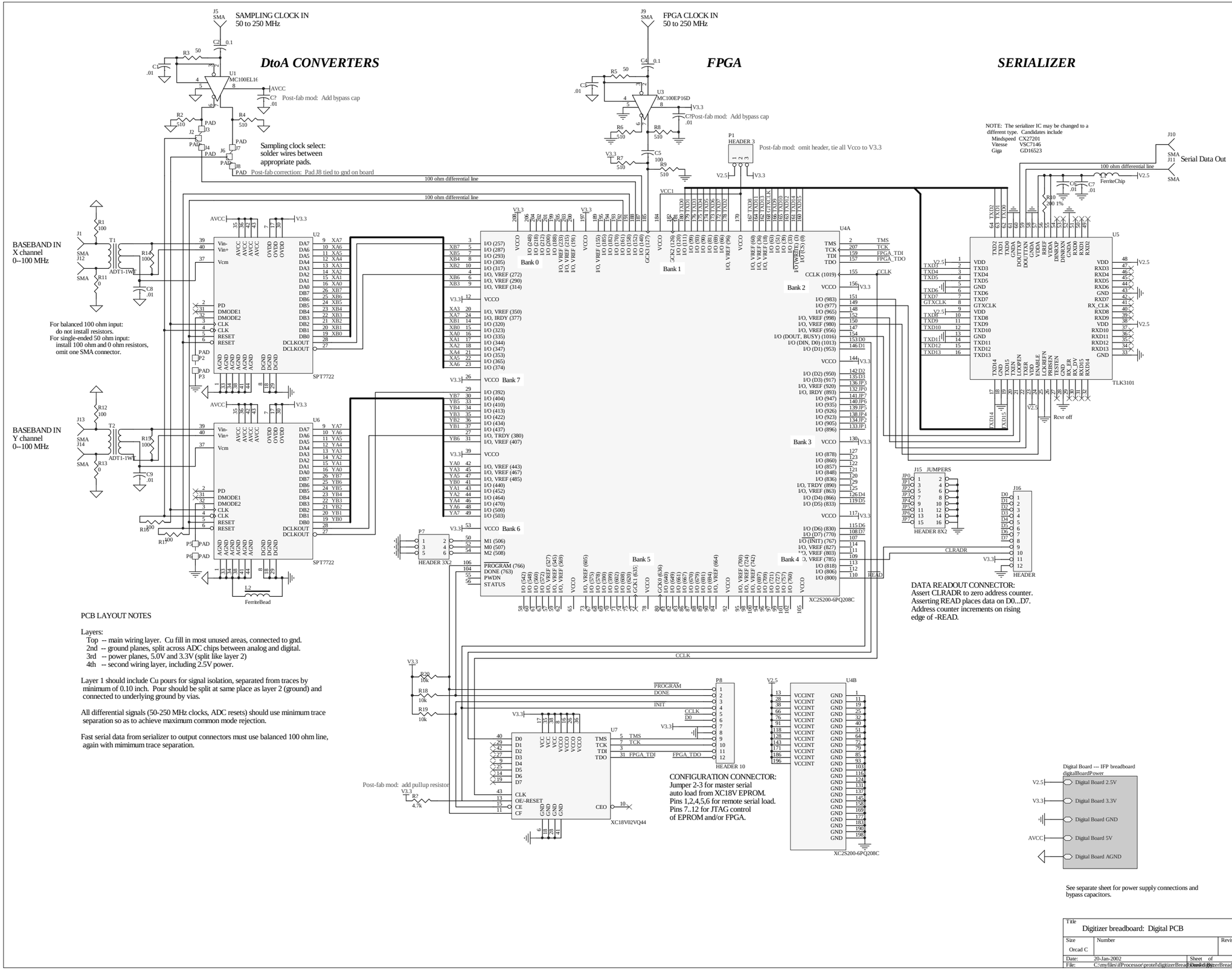


Figure 4: Recommended analog-digital interconnection method


RF IN
1-2 GHz
-20 dBm
J1
SMA
-20 dB RF attenuatiojn
R1 46
R2 0
R3 5
C1 22
C2 22
R4 25
50 ohm microstrip
LO IN
1-2 GHz
-3 dBm
J4
SMA
-5 dB LO
R7 0
R9 35
R8 100
C14 47
C3 47
R10 25
C42 270
U1
RFin
-RFin
LO
-LO
GC
PS_SEL
VccRF
GNDRF
VccLO
GNDLO
Iout
-Iout
Qout
-Qout
PSout
-PSout
VccMxr
GNDMxr
VccPS
GNDPS
GND
Vcc1
Vcc2
Vcc3
MAX2108CEG
VCC
C4 0.1
Vcm
U2
R5 49.9
R6 49.9
AD8131AR
F1 FILTER
F2 FILTER
F3 FILTER
F4 FILTER
IN
GND
OUT
C6 C8 C10 C12
C16 C17 C18 C19
C22 C25 C28 C31
C23 C26 C29 C32
CAP/SM
L1 L2 L3 L4 L5 L6 L7 L8
L9 L10 L11 L12 L13 L14 L15 L16
L17 L19 L21 L23 L25 L27 L29 L31
L18 L20 L22 L24 L26 L28 L30 L32
INDUCTOR
C5 C7 C9 C11 C13
C21 C24 C27 C30 C33
2:1 impedance
T1
T2
ADT2-1T
J2
J3
J5
J7
J8
SMA
U3
UPO
DOUT
REFB
REFA
OUTB
OUTA
VDD
DGND
AGND
OSB
OSA
SCLK
DIN
CS
CL
PDL
MAX5104CEE
C15 0.1
U5
VoutA
VoutB
VDD
GND
SDI
CLK
LOAD
CS
DAC7612
Mod: connect CS to AGND
C43 0.1
C20 0.1
U4
R11 49.9
R12 49.9
AD8131AR
P1
8 HEADER
+5.0 V
C34 10uF
C35 C36 C37 C38 C39 C40
0.1
22
10
R13 2.5k
C41 1.0uF
Vcc3
Vcc2
Vcc1
Vcm
2.5V
U6
+VREF
FB
NC
-VREF
LM336M2.5(8)
Capacitors: Fractional values are in microfarads and integer values are in picofarads unless otherwise noted.
All microstrip lines: 50 ohms characteristic impedance.
Line widths for FR4 (k=4.5):
h=12 mils -> w=20 mils, min line spacing=40
h=20 mils -> w=35 mils , min line spacing=70
h=31 mils -> w=56 mils, min line spacing=100
h=62 mils -> w=114 mils, min line spacing=200
Mount bypass capacitors on top side of board, near corresponding Vcc or Vs pin. With 2 capacitors, put smaller valued one as close as possible to pin.
Title
DIGITIZER BREADBOARD --- ANALOG SECTION
Size
Tabloid
Number
Revision
Date: 20-Jan-2002
Sheet of
File: C:\myfiles\ifProcessor\protel\digitizerBreadboard\digitizerBreadboard.ddb
Drawn by:



PCB LAYOUT NOTES

Layers:
- Top -- main wiring layer. Cu fill in most unused areas, connected to gnd.
- 2nd -- ground planes, split across ADC chips between analog and digital.
- 3rd -- power planes, 5.0V and 3.3V (split like layer 2)
- 4th -- second wiring layer, including 2.5V power.

Layer 1 should include Cu pours for signal isolation, separated from traces by minimum of 0.10 inch. Pour should be split at same place as layer 2 (ground) and connected to underlying ground by vias.

All differential signals (50-250 MHz clocks, ADC resets) should use minimum trace separation so as to achieve maximum common mode rejection.

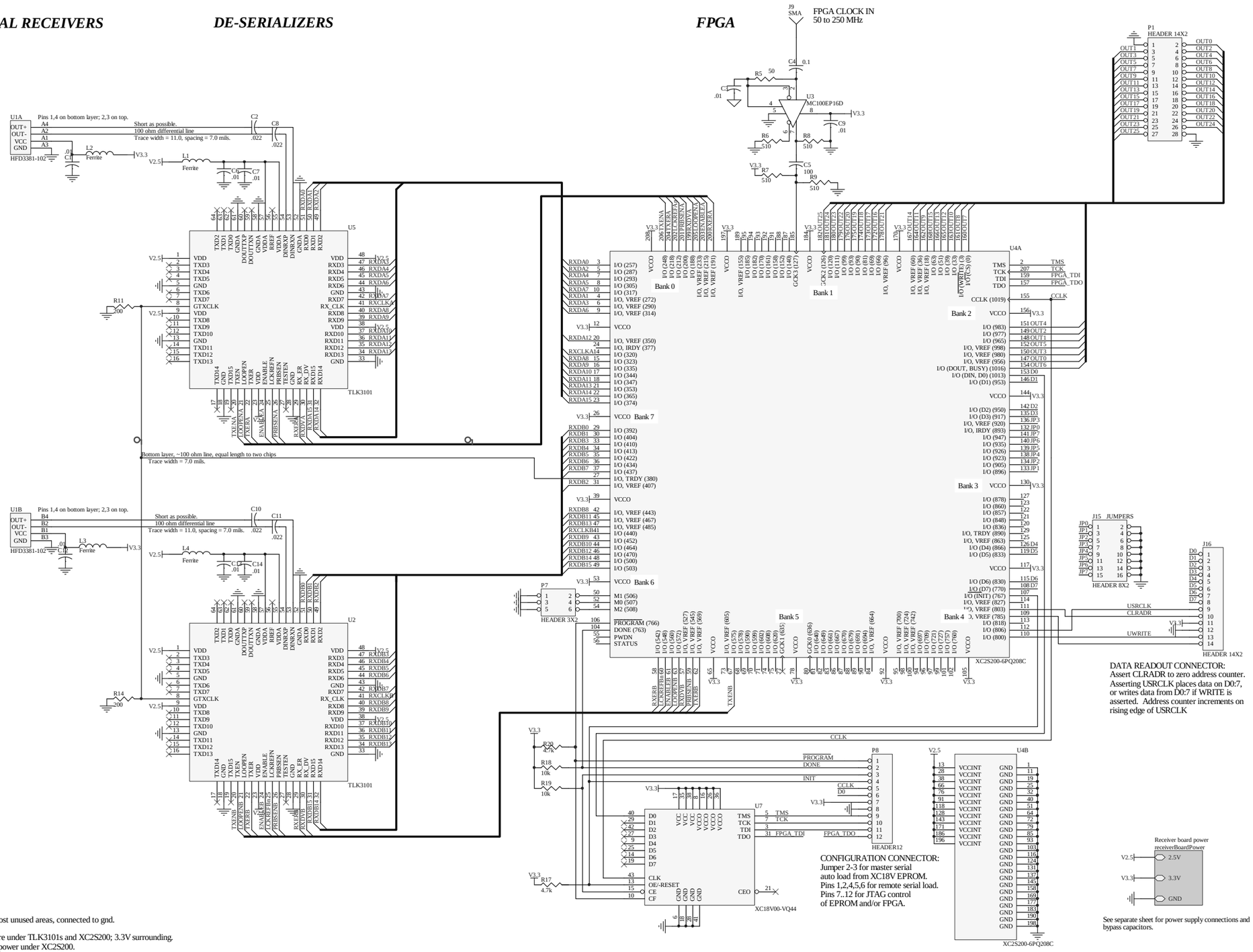
Fast serial data from serializer to output connectors must use balanced 100 ohm line, again with mimimum trace separation.

Title: Digitizer breadboard: Digital PCB		
Size: Orcad C	Number	Revision
Date: 20-Jan-2002	Sheet of	
File: C:\myfiles\dProcessor\protel\digitizerBreadboard\DigitizerBreadboard.ddb	Drawn by:	

OPTICAL RECEIVERS

DE-SERIALIZERS

FPGA



PCB LAYOUT NOTES

Layers:
- Top -- main wiring layer. Cu fill in most unused areas, connected to gnd.
- 2nd -- ground plane
- 3rd -- power plane, 2.5V center square under TLK3101s and XC2S200; 3.3V surrounding.
- 4th -- second wiring layer, incl 3.3V power under XC2S200.

Layer 1 should include Cu pours for signal isolation, separated from traces by minimum of 0.10 inch. Pour should be split at same place as layer 2 (ground) and connected to underlying ground by vias.

All differential signals (50-250 MHz clocks, ADC resets) should use minimum trace separation so as to achieve maximum common mode rejection.

Fast serial data must use balanced 100 ohm line, again with mimimum trace separation.

Title: Receiver breadboard, PCB schematic		
Size: Orcad C	Number:	Revision:
Date: 20-Jan-2002	Sheet of	
File: C:\myfiles\fProcessor\protel\receiverBreadboard.ddb	Drawn By:	