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THE ATA IMAGER UPDATE

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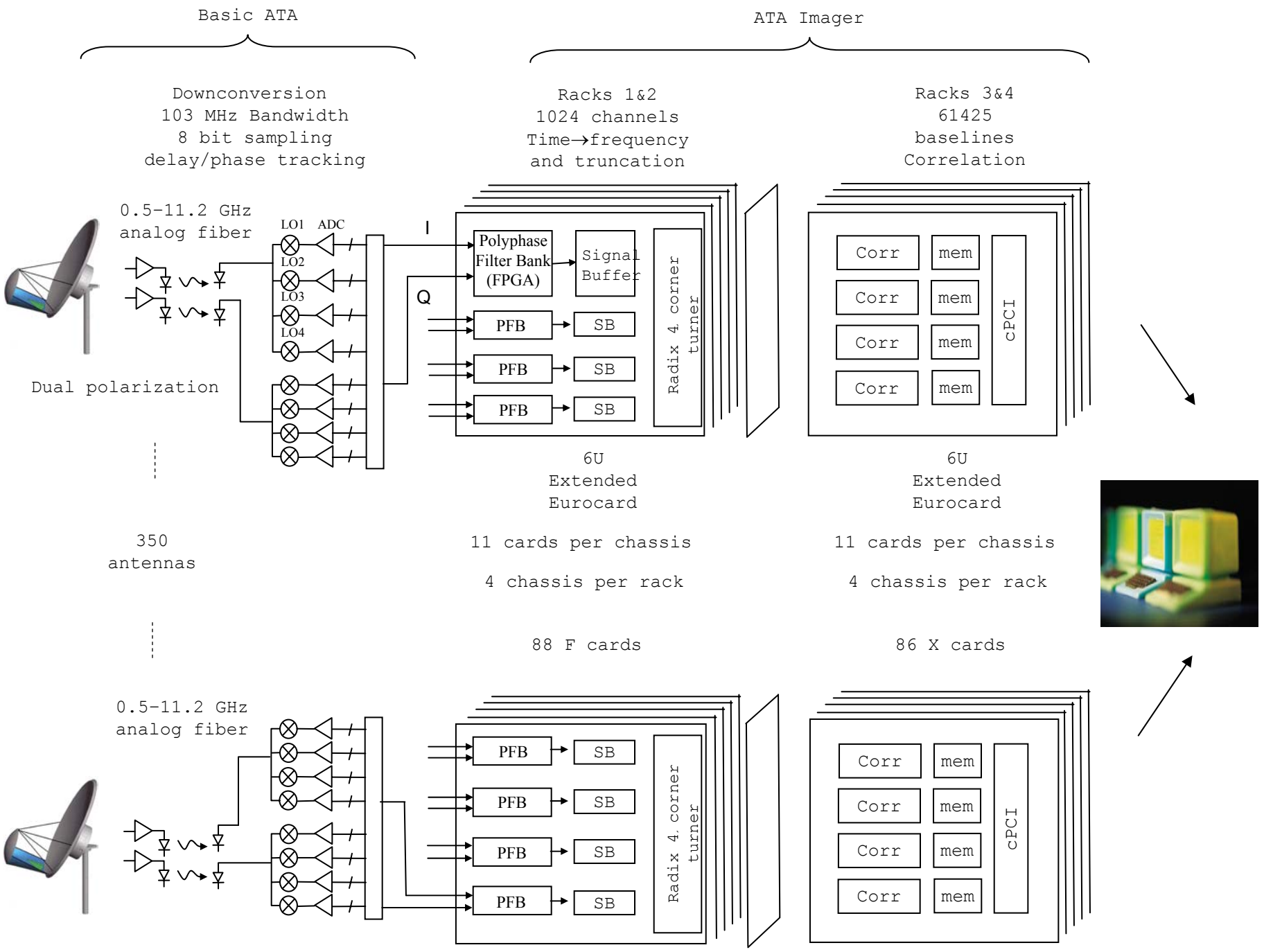
The Allen Telescope Array will be a unique instrument in its ability to conduct several experiments at once. It will have the ability to observe in several independent directions within the primary beam of the individual antennas. Four 100 MHz dual polarization IFs can be independently tuned to anywhere within the .5 to 11.2 GHz RF band of the front end. SETI searches, pulsar experiments and imaging can be conducted at the same time. All tuning and pointing functions including fringe stopping and delay compensation are provided by the array for all of the instruments that will use it. The ATA imager is one of those instruments and will have two 100 MHz IF ports available to it for a total bandwidth capability of 200 MHz. A modest prototype correlator for only 4 antennas has been developed in order to test various concepts and to develop VHDL code that will be used in the 350 antenna version. It is a 100 MHz correlator in an FX architecture with 1024 frequency channels and it measures all 4 Stokes parameters.

Currently three 6-meter antennas have been installed and should be fully functional at the time of this meeting. The prototype correlator will be used to help test out the system. By September of 2004 we expect to have 32 antennas. The current plan is to build a 32 antenna correlator system designed to be expandable to 350 antennas. The correlator will be expanded in steps as the array grows. The current status of the imaging back end will be discussed.

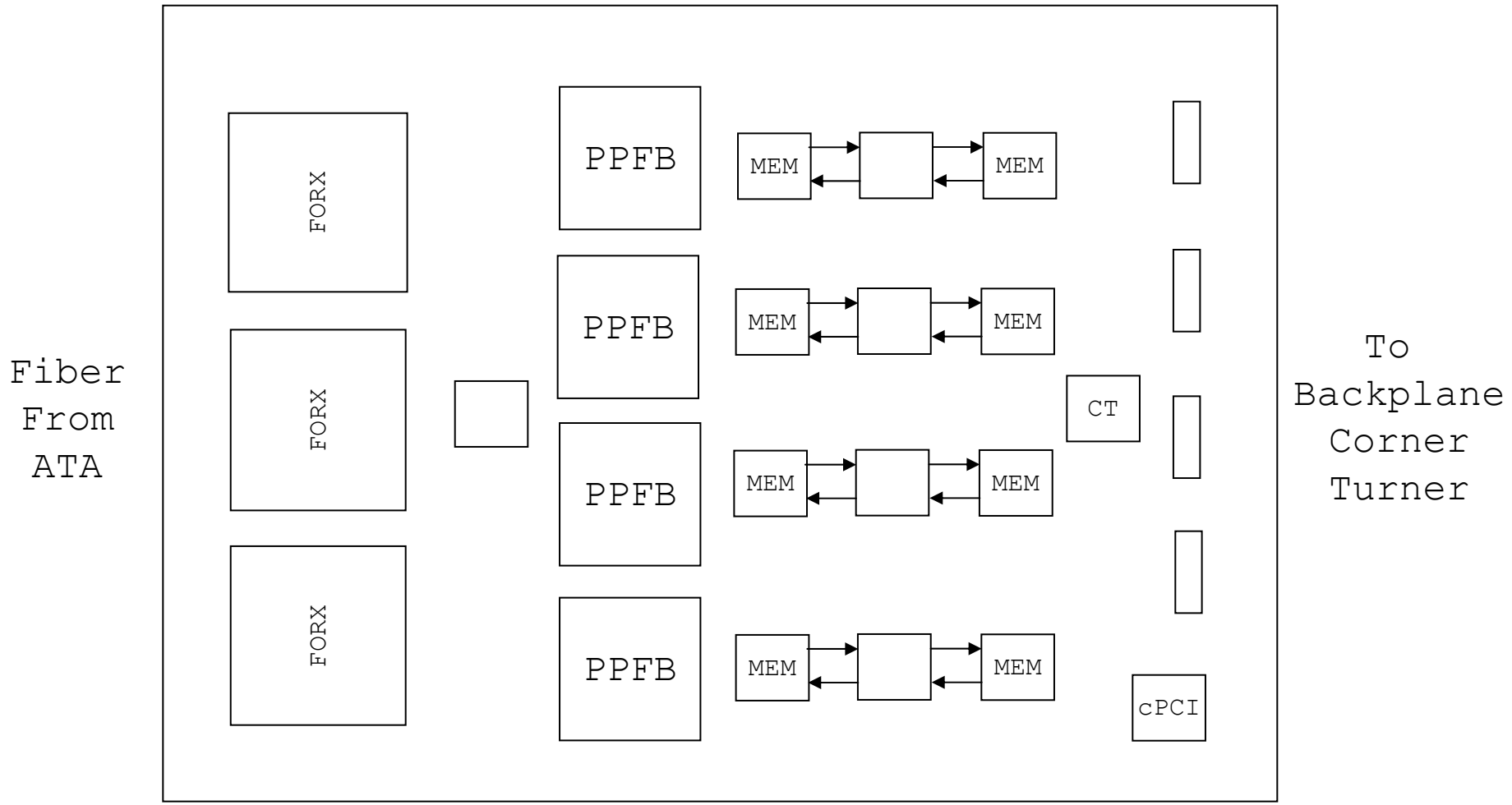
As I presented at this conference two years ago, the ATA imager relies on an FX correlator architecture. In order to avoid the severe channel to channel sidelobes produced by using the FFT as a filterbank, a polyphase technique is used. The severe problem of distributing the signals from the polyphase filterbank to the correlator is solved by using a corner turner of unique design which converts the 350 streams of 1024 channels into 350 streams of antennas of 3 frequency channels each. Each correlator is presented with a sequential stream of all of the

antennas where all 61425 baselines are computed as the data enters one antenna at a time.

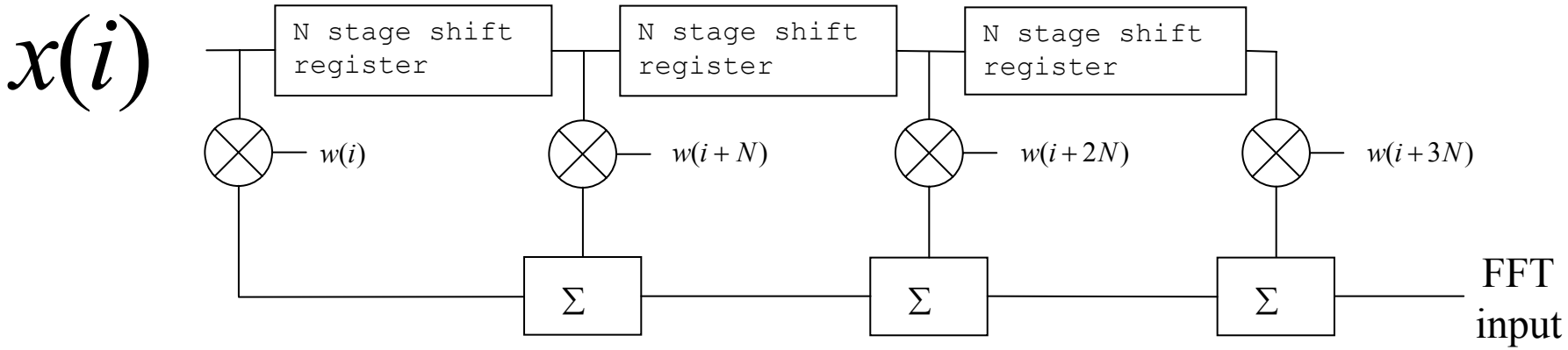
There have been some changes to the architecture of the correlator since I last presented it at this conference two years ago. One innovation enables us to replace a significant amount expensive FPGA memory with less expensive off chip memory while preserving the basic idea of a pipeline correlator with low chip to chip wiring and easy expandability. This innovation requires the use of inexpensive memory as a signal buffer to reorder the frequency channel samples as they emerge from the polyphase filter bank. The large memory signal buffer also enables us to gain a great deal of flexibility in our implementation of the switched corner turner. The modifications required to a corner turner as the system is expanded will be discussed.


Basic ATA
ATA Imager
Downconversion
103 MHz Bandwidth
8 bit sampling
delay/phase tracking
Racks 1&2
1024 channels
Time→frequency
and truncation
Racks 3&4
61425
baselines
Correlation
0.5–11.2 GHz
analog fiber
LO1
ADC
LO2
LO3
LO4
I
Q
Polyphase
Filter Bank
(FPGA)
Signal
Buffer
PFB
SB
Radix 4 corner
turner
Corr
mem
cPCI
Dual polarization
6U
Extended
Eurocard
11 cards per chassis
4 chassis per rack
88 F cards
86 X cards
350
antennas
0.5–11.2 GHz
analog fiber

F Card

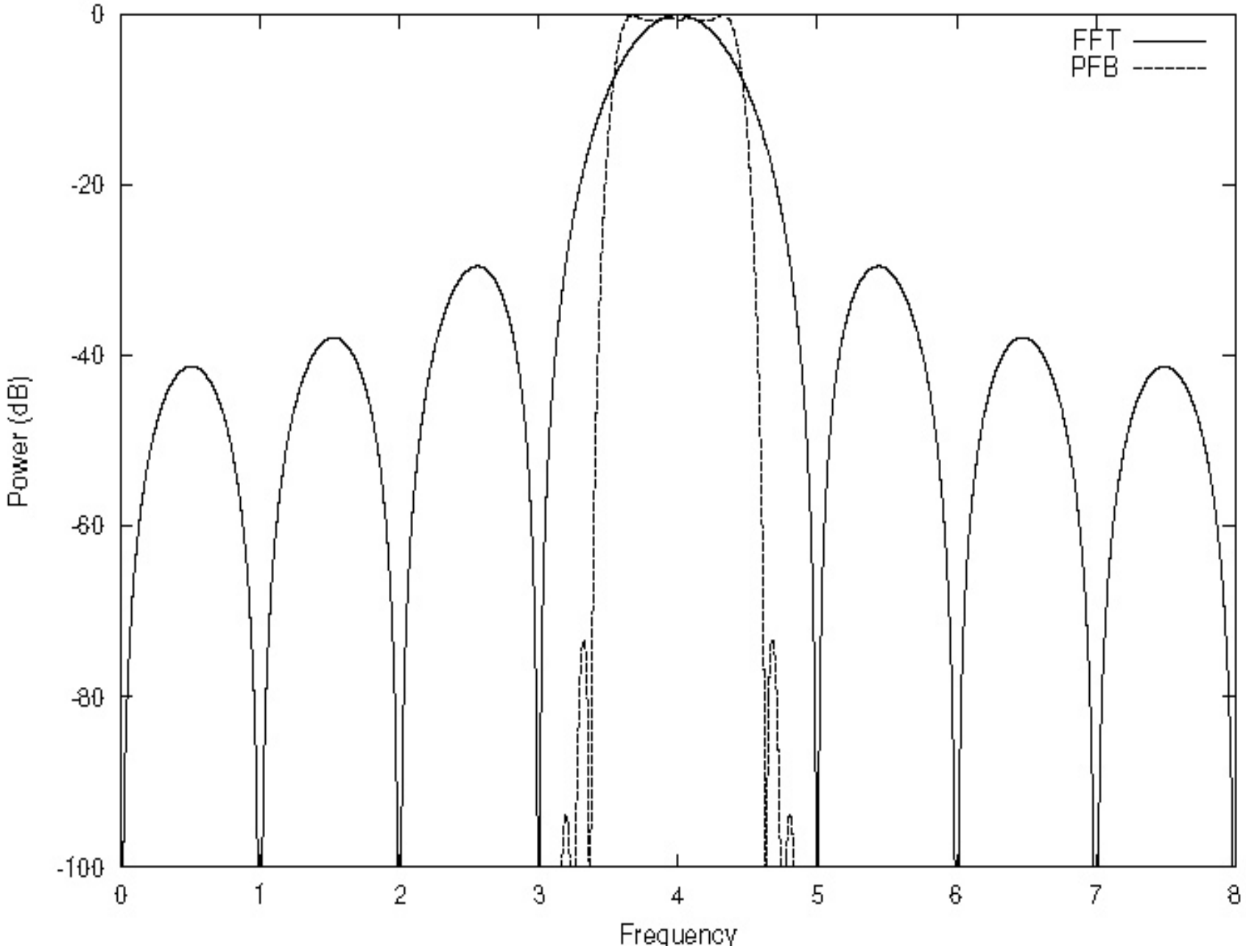

Fiber From ATA
FORX
FORX
FORX
PPFB
PPFB
PPFB
PPFB
MEM
MEM
MEM
MEM
MEM
MEM
MEM
MEM
CT
cPCI
To Backplane Corner Turner

$$S(f) = \frac{1}{N}\sum_{i=0}^{N-1} w(i)x(i)e^{-j2\pi if/N}$$

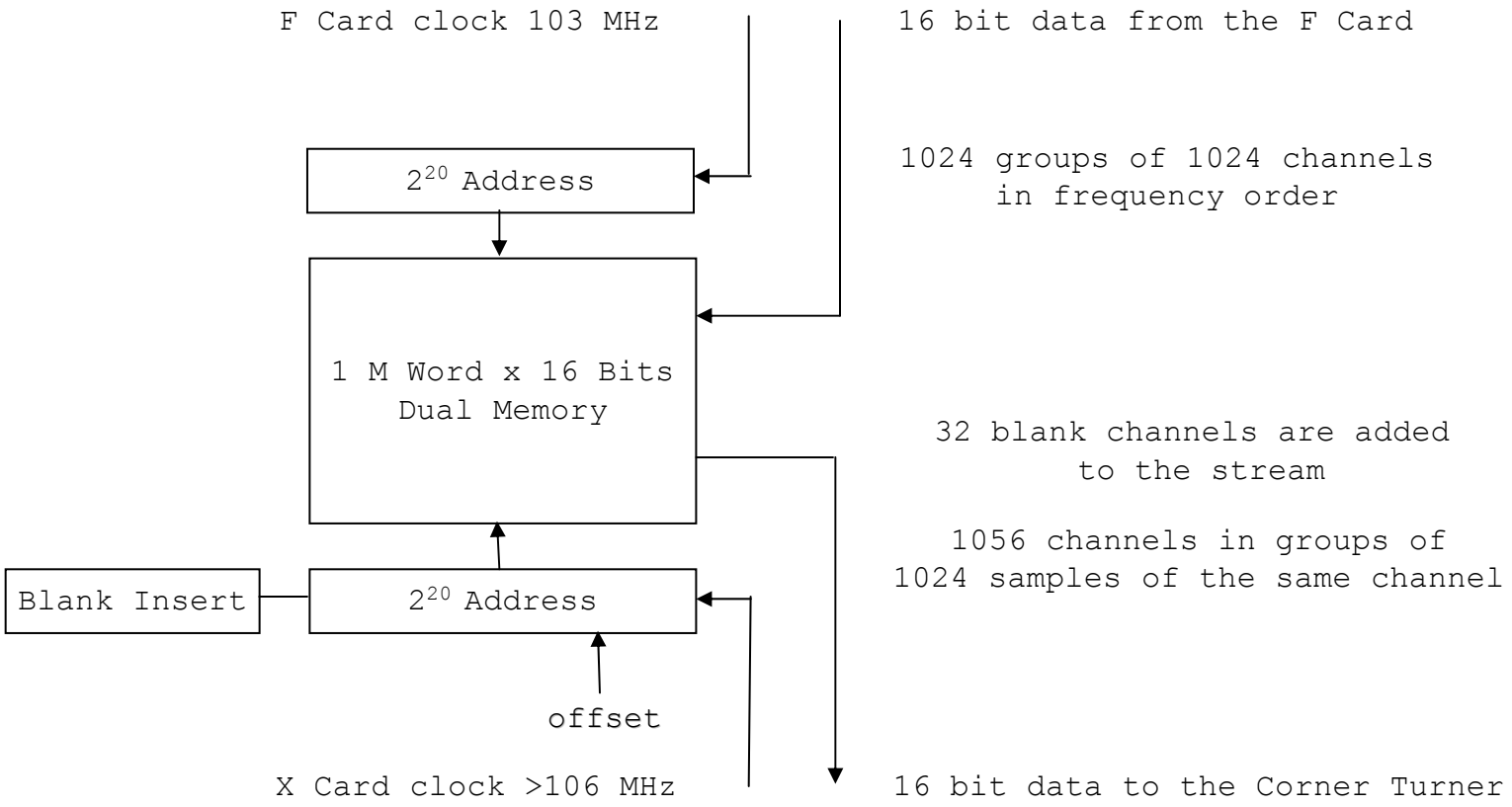


$$S(f) = \frac{1}{N}\sum_{i=0}^{N-1}\left(\sum_{a=0}^{b} w(i+aN)\,x(i+aN)\right)e^{-j2\pi if/N}$$

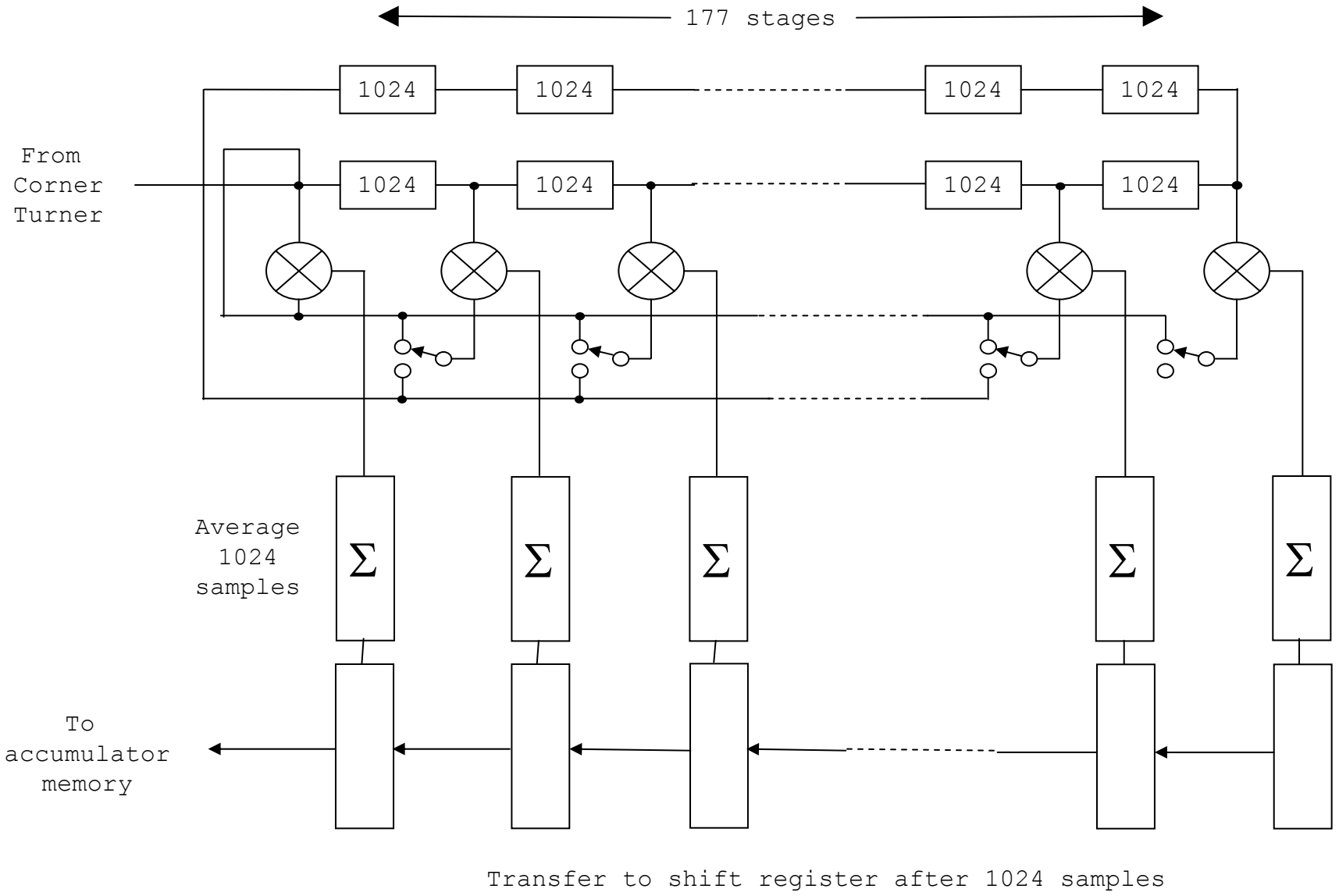
Polyphase filter bank expression


FFT
PFB
Power (dB)
Frequency
0
-20
-40
-60
-80
-100
0
1
2
3
4
5
6
7
8

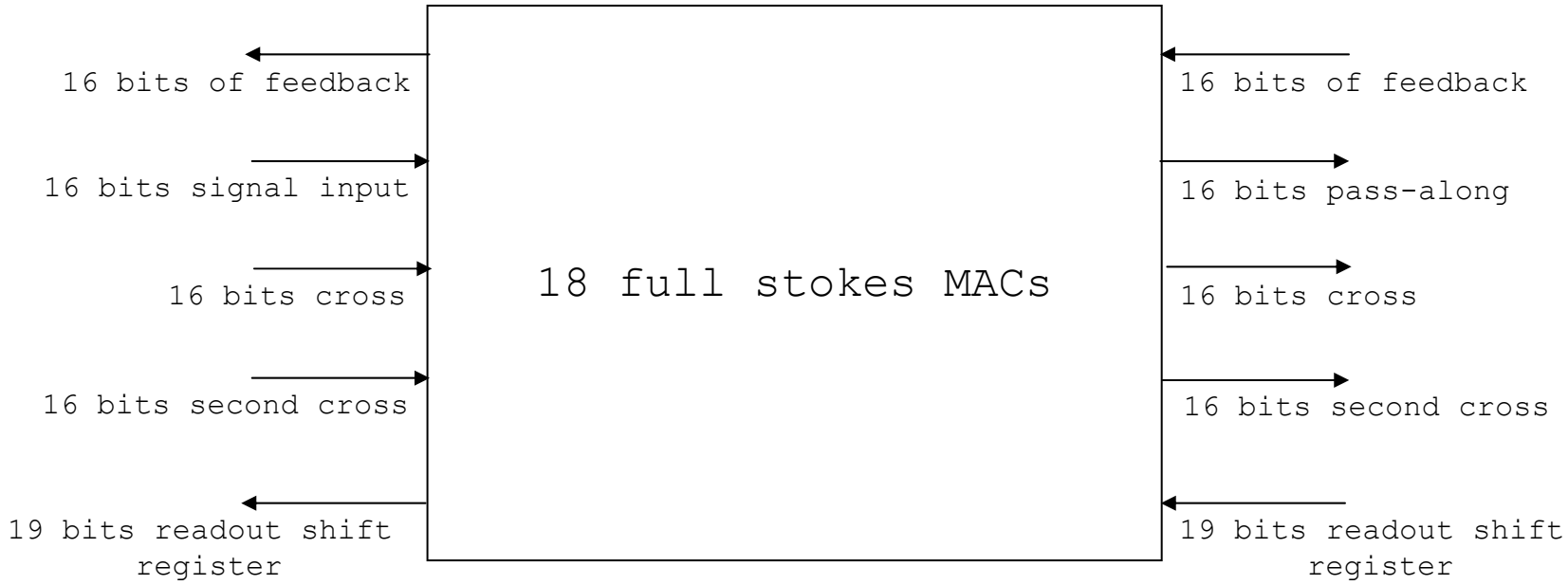
Signal Buffer



Correlator


177 stages
1024
1024
1024
1024
1024
1024
1024
1024
From
Corner
Turner
Average
1024
samples
Σ
Σ
Σ
Σ
Σ
To
accumulator
memory
Transfer to shift register after 1024 samples

Single FPGA chip layout

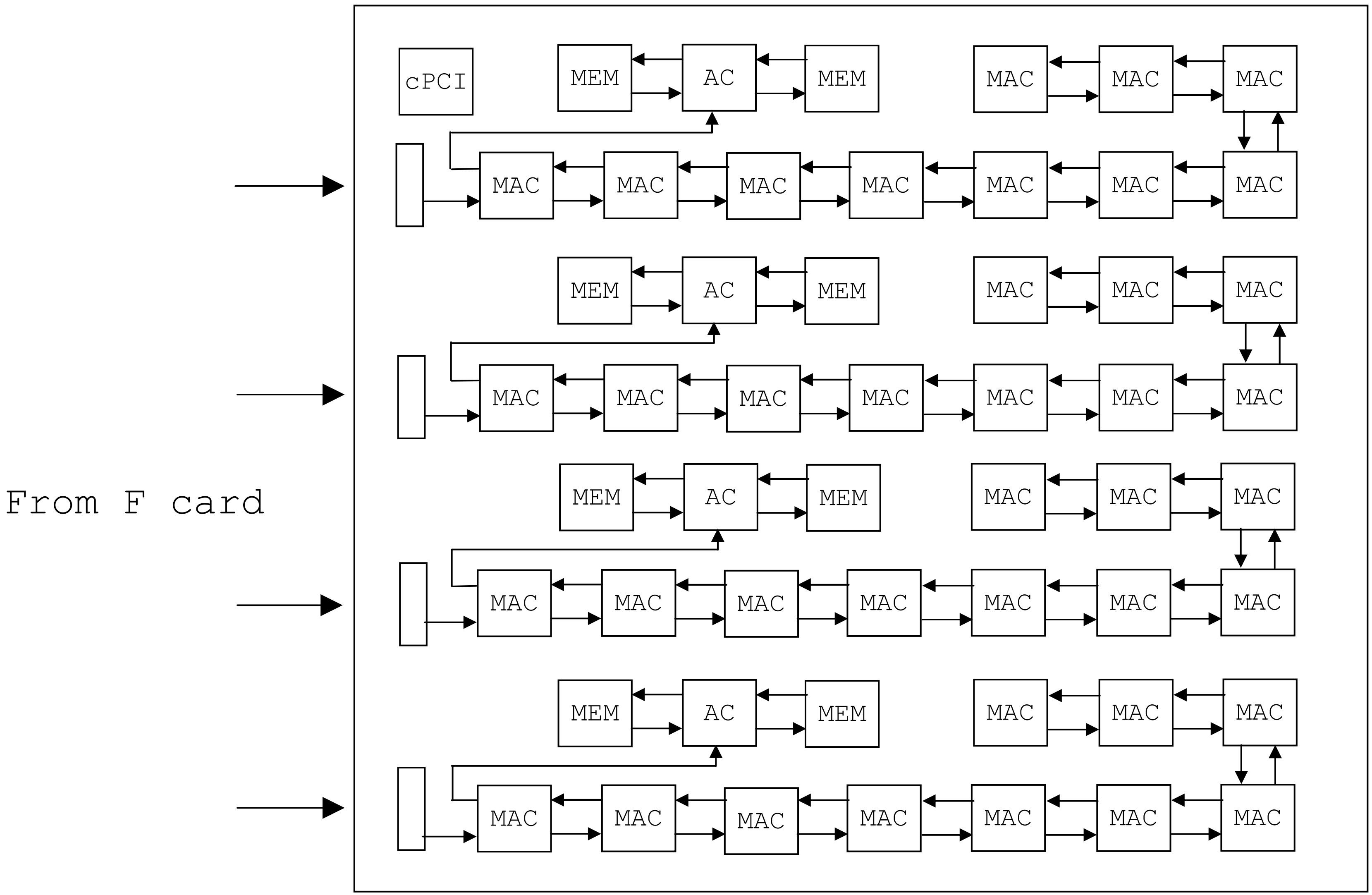


Spartan III or Virtex II 1000 series FT256 package

Virtex II 40 18 bit multipliers 40 18 by 1024 RAM

Spartan III 24 18 bit multipliers 24 18 by 1024 RAM

X Card


From F card
cPCI
MEM
AC
MEM
MAC
MAC
MAC
MAC
MAC
MAC
MAC
MAC
MAC
MAC